36 V, Low Power, High Precision Op Amp

Features

- Low Offset Voltage:
  10 μV max (B Grade)
  20 μV max (A Grade)
- Low Offset Voltage Temperature Drift:
  0.5 μV/°C max (B Grade)
  1.0 μV/°C max (A Grade)
- Low Input Bias Current: 25 pA max
- Low Noise Density: 10 nV/$\sqrt{Hz}$ (f=1 kHz)
- Low Noise: 0.8 μV_{P-P} (f=0.1~10 Hz)
- Input Voltage Range Extends to Negative Power Supply
- CMRR: 120 dB min
- PSRR: 120 dB min (full temperature range)
- A_{VOL}: 120 dB min (full temperature range)
- Supply Current: 500 μA/amplifier
- Gain Bandwidth Product: 1.3 MHz, unit gain stable
- Single/dual Power Supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- Specified Temperature Range: -40 °C to +125 °C

Applications

- Precision data acquisition
- Instrumentation
- Sensor signal conditioning
- Industrial control
- Optical communication
- Smart grid

General Description

ZJA3008 series high-precision continuous operational amplifiers featuring lower than 10 μV offset voltage, better than 0.5 μV/°C offset voltage drift, 25 pA input bias current and 10 nV/$\sqrt{Hz}$ low noise. These features make them exceptionally suitable for precision signal conditioning, such as precision sensor interface, voltage amplification, current to voltage conversion and filtering.

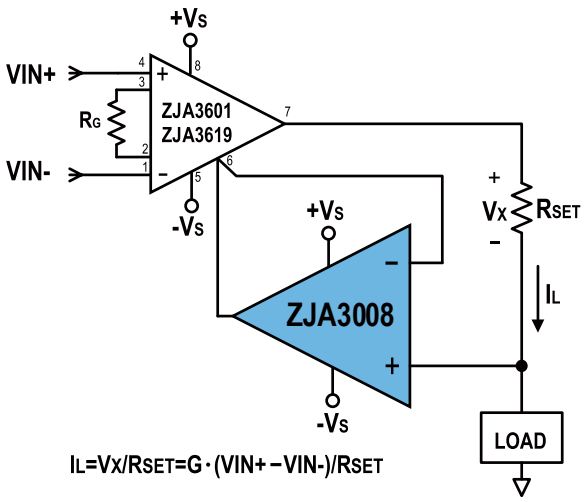
The ZJA3008 has a low supply current of 500 μA per channel, making them suitable for applications with strict requirements on power consumption or heat management, such as 4-20 mA loop powered instruments.

ZJA3008's input bias current is better than 25 pA, the offset voltage is better than 10 μV, the offset voltage temperature drift is better than 0.5 μV/°C, and the input range extends to the negative power rail. This makes ZJA3008 very suitable for the sensor signal conditioning, whether in single-supply or dual-supply designs. ZJA3008 can also simplify the entire process of sensor conditioning modules' manufacturing.

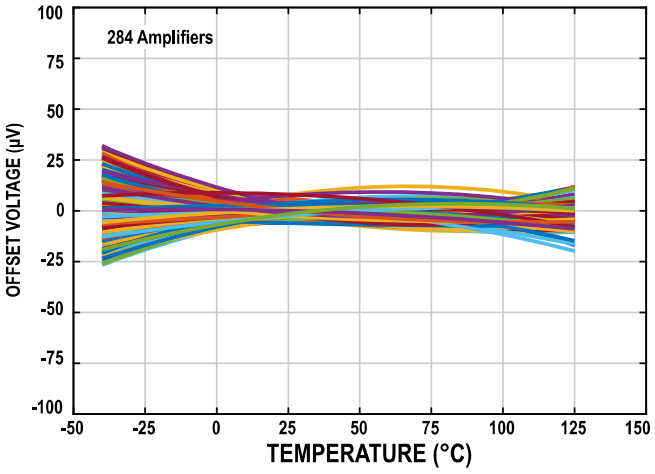
The ZJA3008 has a wide power supply voltage range, operating from ±2.25 V to ±18 V for dual-supply operation or 4.5 V to 36 V for single-supply. It further expands its input capabilities to negative rail, making it ideal for a variety of applications.

ZJA3008-2 is dual channel part and offered in a 8-lead SOIC and a 8-lead MSOP package.

Application Examples



Typical Performance Characteristics



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Version (Release A) [1]

Revision History

August 2024——Release A

[1] Information furnished by ZJW Microelectronics is believed to be accurate and reliable. However, no responsibility is assumed by ZJW Microelectronics for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of ZJW Microelectronics. Trademarks and registered trademarks are the property of their respective owners.

Pin Configurations and Function Descriptions

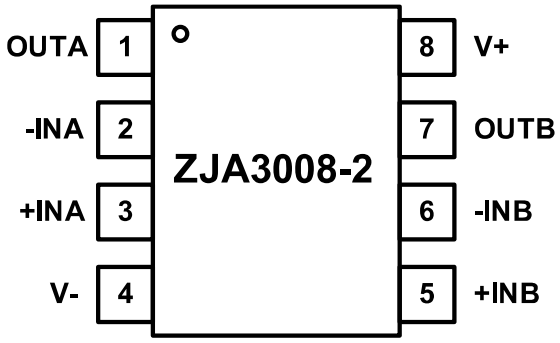

Figure 1. ZJA3008-2 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O [1]	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
V-	4	P	Negative power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
V+	8	P	Positive power supply

[1] AI: Analog Input; P: Power; AO: Analog Output.

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	40 V
Input Voltage	$\pm V_{SY}$
Input Current [2]	±10 mA
Differential Input Voltage	$(+V_{SY})-(-V_{SY})$
Output Short-Circuit Duration to GND [3]	Continuous
Operating Temperature Range	-40 °C to +125 °C
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature Range	-65 °C to +150 °C
Maximum Reflow Temperature [4]	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
Electrostatic Discharge (ESD) [5]	
Human Body Model (HBM) [6]	750 V
Charged Device Model (CDM) [7]	1000 V

Thermal Resistance [8]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-8	158	43	°C/W
MSOP-8	190	44	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] There are clamping diodes between the input pins and the power pins, and also between each other. When the input signal exceeds the supply rail by 0.3 V, the input current is limited to 10 mA.

[3] Limited by Over Temperature Protection (OTP).

[4] IPC/JEDEC J-STD-020 Compliant

[5] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[6] ANSI/ESDA/JEDEC JS-001 Compliant

[7] ANSI/ESDA/JEDEC JS-002 Complaint

[8] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at V_S=±15 V, V_{CM}=0 V, T_A=25 °C.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	B Grade			2.5	10	μV
			●			65	μV
		A Grade			5	20	μV
			●			130	μV
Offset Voltage Drift	TCV_{OS}	B Grade	●		0.25	0.5	μV/°C
		A Grade	●		0.5	1.0	μV/°C
Input Bias Current	I_B				5	25	pA
			●			10	nA
Input Offset Current	I_{OS}				2	10	pA
			●			2	nA
Input voltage range	IVR			-15		12	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=-15.0 V to 12 V		120	130		dB
			●	114			dB
		V_{CM}=-15.0 V to 12.5 V		114	124		dB
			●	108			dB
Open-Loop Voltage Gain	A_{VOL}	R_L=10 kΩ, Vo=±14.5 V		126	140		dB
			●	120			dB
		R_L=2 kΩ, Vo=±13.0 V		126	140		dB
			●	120			dB
Input resistance/capacitance	R_{IN}/C_{IN}	Differential Mode			TBD		GΩ/pF
		Common Mode			TBD		TΩ/pF
OUTPUT CHARACTERISTICS							
Output Voltage (High)	V_{OH}	R_L=10 kΩ			100	200	mV
			●			300	mV
		R_L=2 kΩ			500	1000	mV
			●			1500	mV
Output Voltage (Low)	V_{OL}	R_L=10 kΩ			50	100	mV
			●			150	mV
		R_L=2 kΩ			250	500	mV
			●			750	mV
Short-Circuit Current	I_{SC}				25		mA

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
POWER SUPPLY							
Supply Current (per Amplifier)	I_{SY}	V_O=0 V			500	525	μA
			●		667	700	μA
Power Supply Rejection Ratio	PSRR	V_{SY}=±3 V to ±18 V		126	140		dB
			●	120			dB
DYNAMIC PERFORMANCE							
Slew Rate	SR	R_L=2 kΩ			0.9		V/μs
Gain Bandwidth Product	GBP	R_L=2 kΩ, G=100, V_{IN}=100 mV_{P-P}			1.3		MHz
-3 dB Bandwidth	-3 dB BW	R_L=2 kΩ, G=1, V_O=100 mV_{P-P}			3.4		MHz
Settling Time	t_S	to 0.1%, G=-1, 0 to 10 V step			15		μs
		to 0.01%, G=-1, 0 to 10 V step			16		μs
Overload Recovery Time	t_{OR}	R_L=10 kΩ, G=-10, VIN=±2 V step			2		μs
Total Harmonic Distortion + Noise	THD+N	R_L=2 kΩ, G=1, f=1 kHz, V_O=3.5 Vrms			-112		dB
Phase Margin	PM	R_L=2 kΩ, G=1, VIN=100 mV_{P-P}			57		°
Multiple Amplifier Channel Separation	C_S	R_L=10 kΩ, f=1 kHz			-120		dB
NOISE PERFORMANCE							
Voltage Noise	$e_{n,P-P}$	0.1 Hz to 10 Hz			0.8		$μV_{P-P}$
Voltage Noise Density	e_n	f=1 kHz			10		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f=1 kHz			2		$fA/\sqrt{Hz}$
OVER TEMPERATURE PROTECTION							
Trigger Temperature	T_{IN}				150		°C
Exit Temperature	T_{EXIT}				130		°C
TEMPERATURE RANGE		Specified Temperature Range		-40		125	°C

Typical Performance Characteristics

Unless otherwise stated, V_{SY} =±15.0 V, V_{CM}=0 V, T_A=25 °C.

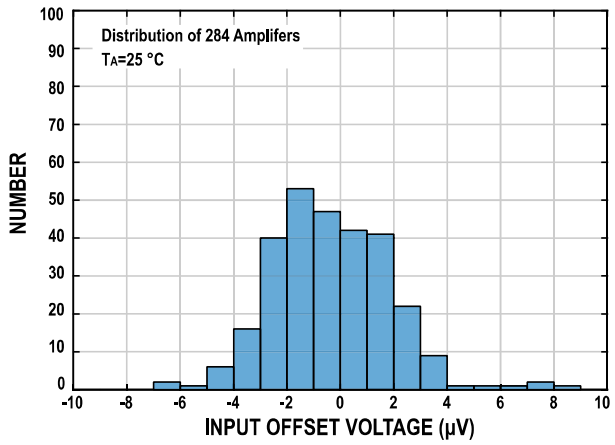

Figure 2. Input Offset Voltage Distribution at 25 °C

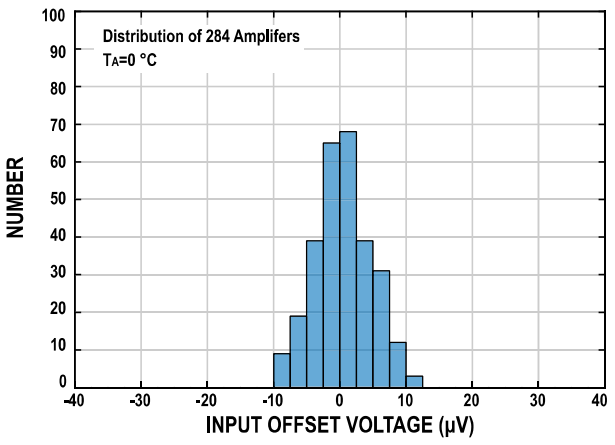

Figure 3. Input Offset Voltage Distribution at 0 °C

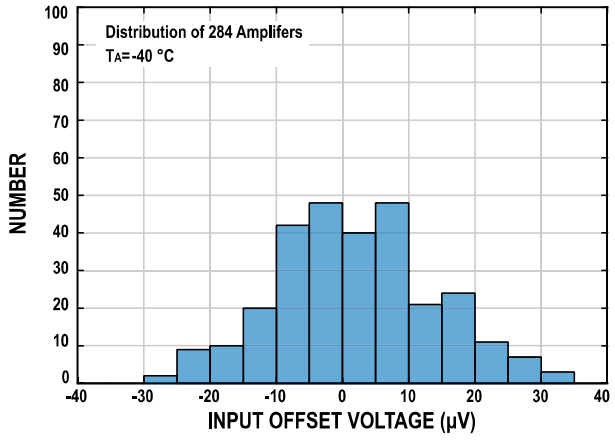

Figure 4. Input Offset Voltage Distribution at -40 °C

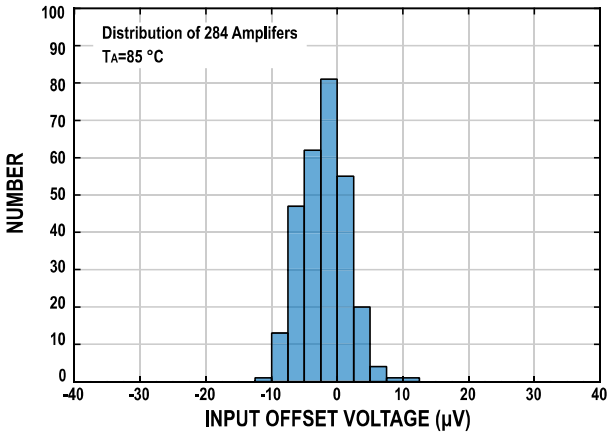

Figure 5. Input Offset Voltage Distribution at 85 °C

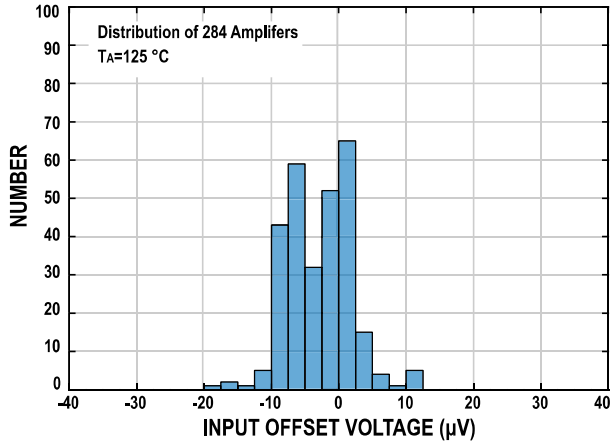

Figure 6. Input Offset Voltage Distribution at 125 °C

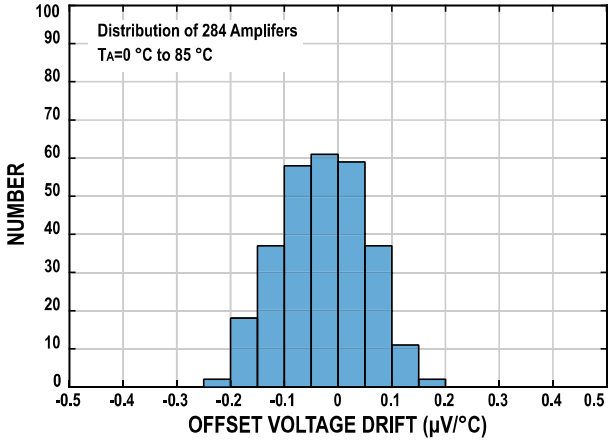

Figure 7. Offset Voltage Drift Distribution (0 °C to 85 °C)

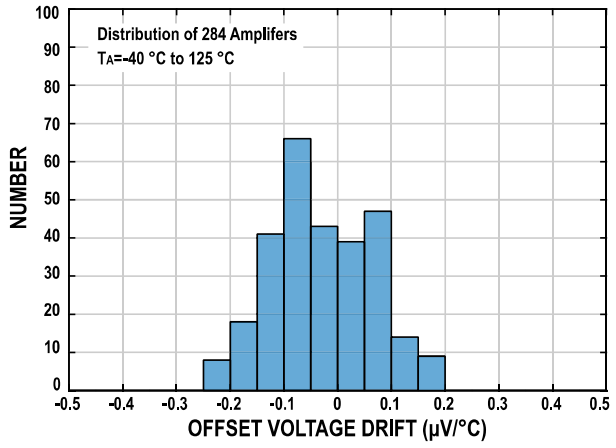

Figure 8. Offset Voltage Drift Distribution (-40 °C to 125 °C)

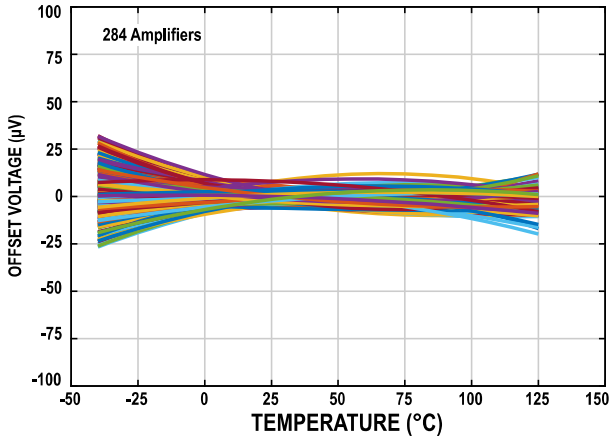

Figure 9. Input Offset Voltage vs. Temperature

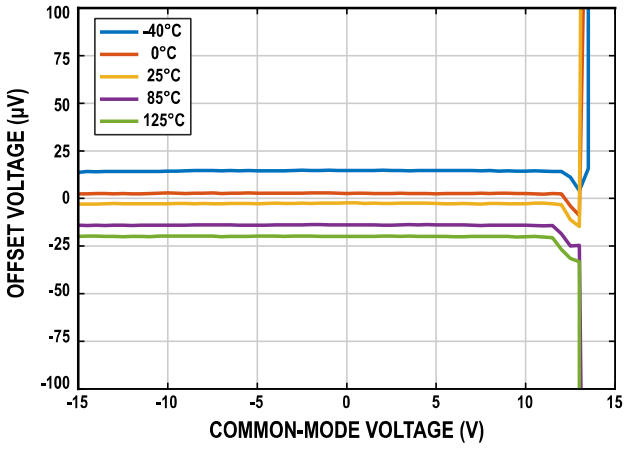

Figure 10. Offset Voltage vs. Common-Mode Voltage

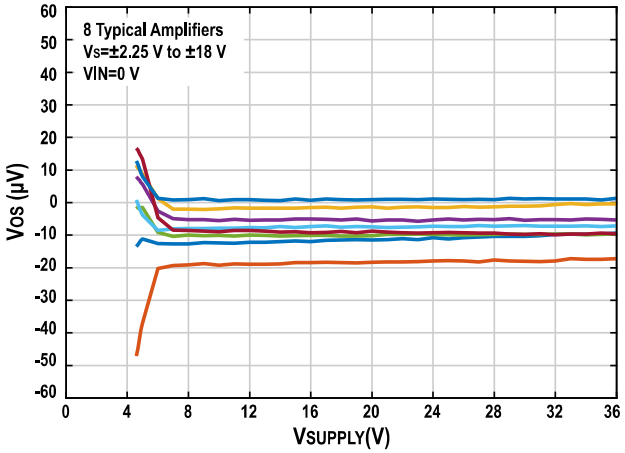

Figure 11. Offset Voltage vs. Power Supply, VIN=0 V

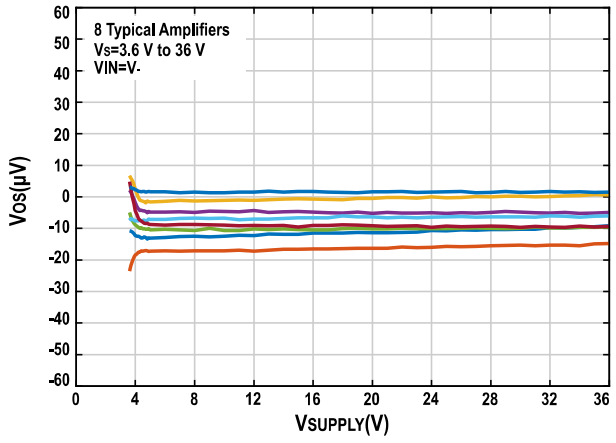

Figure 12. Offset Voltage vs. Power Supply, VIN=V-

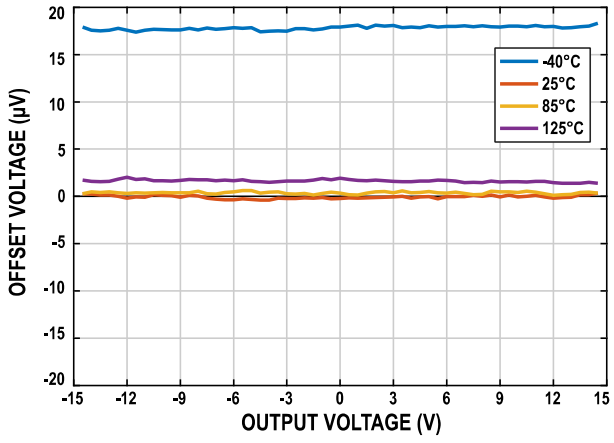

Figure 13. Offset Voltage vs. Output Voltage, R_L=10 kΩ

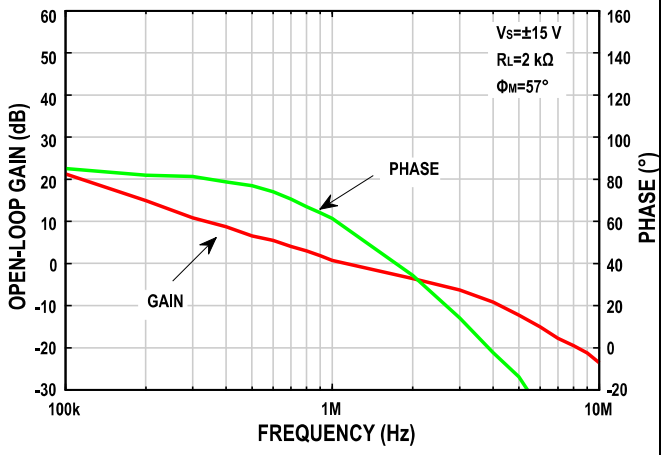

Figure 14. Open-Loop Gain and Phase vs. Frequency

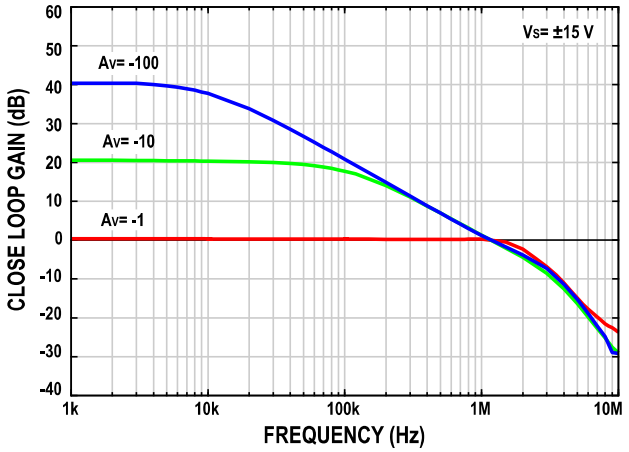

Figure 15. Closed-Loop Gain vs. Frequency

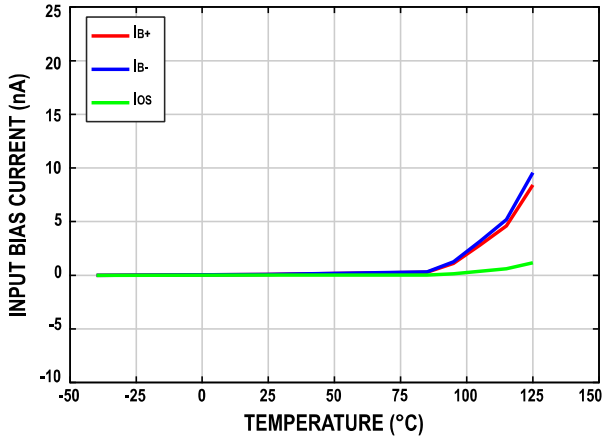

Figure 16. Input Bias Current vs. Temperature

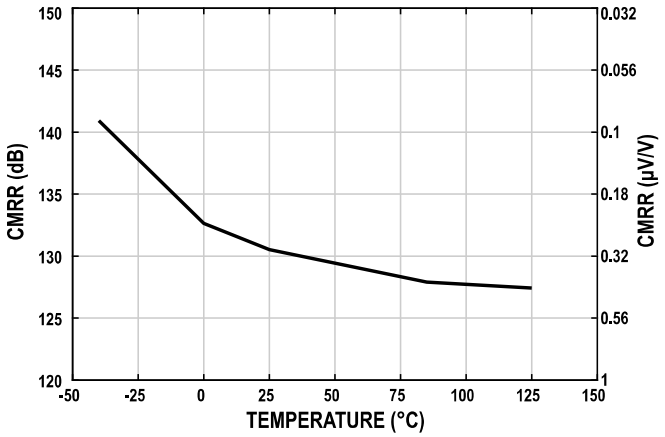

Figure 17. Common Mode Rejection Ratio (CMRR) vs. Temperature

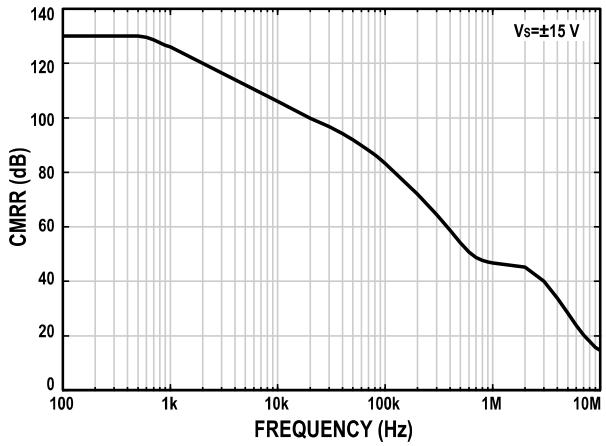

Figure 18. Common Mode Rejection Ratio (CMRR) vs. Frequency

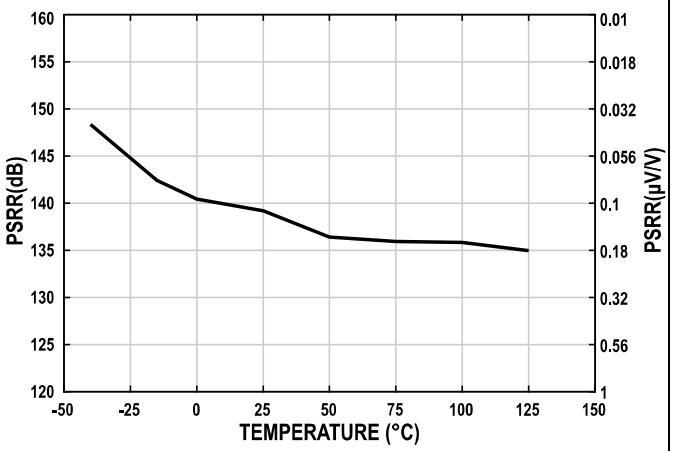

Figure 19. Power Supply Rejection Ratio (PSRR) vs. Temperature

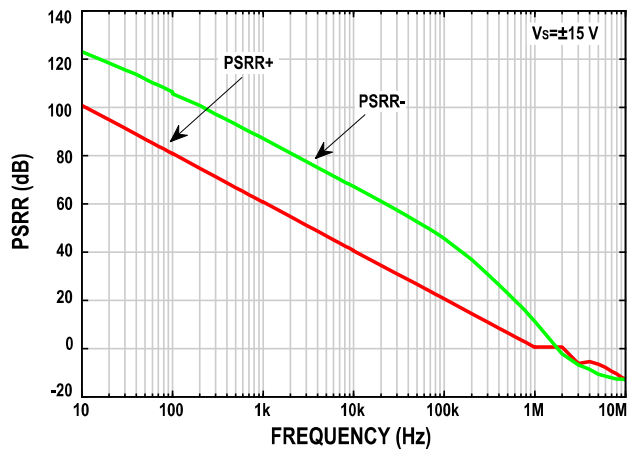

Figure 20. Power Supply Rejection Ratio (PSRR) vs. Frequency

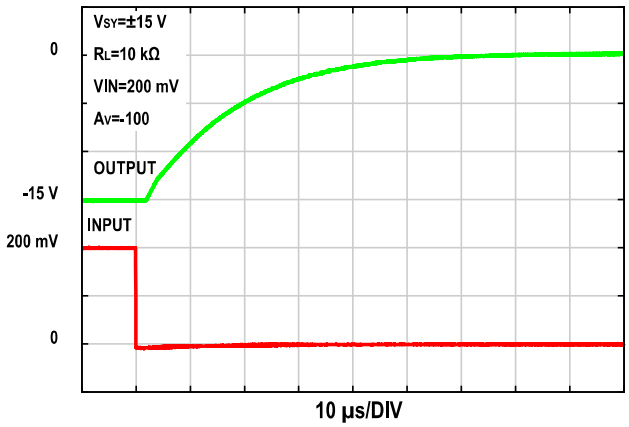

Figure 21. Positive Overload Recovery

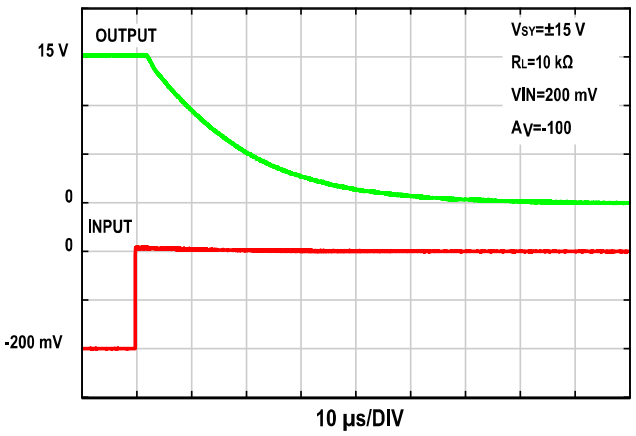

Figure 22. Negative Overload Recovery

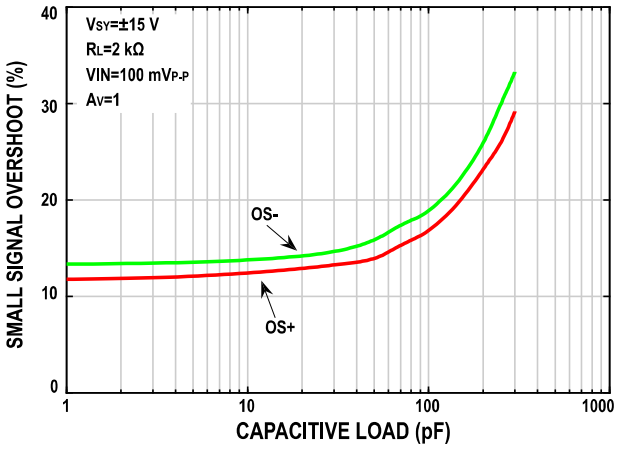

Figure 23. Small-Signal Overshoot vs. Capacitive Load

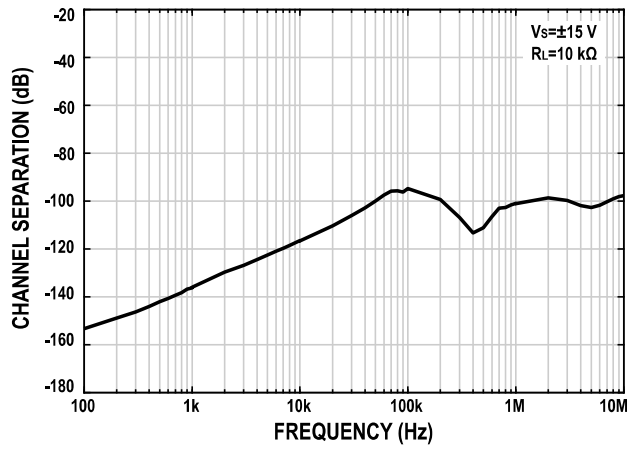

Figure 24. Channel Separation vs. Frequency

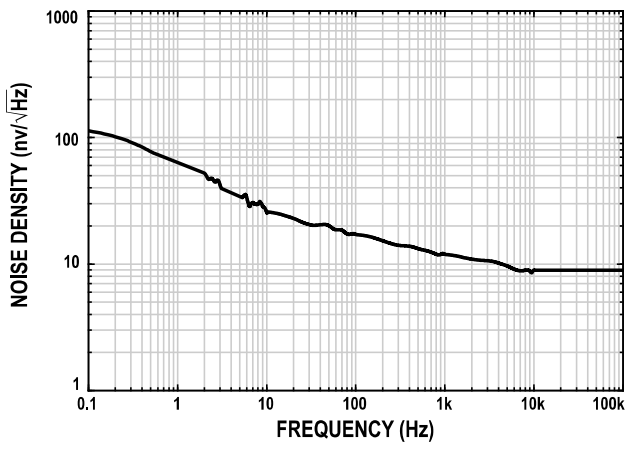

Figure 25. Voltage Noise Density vs. Frequency

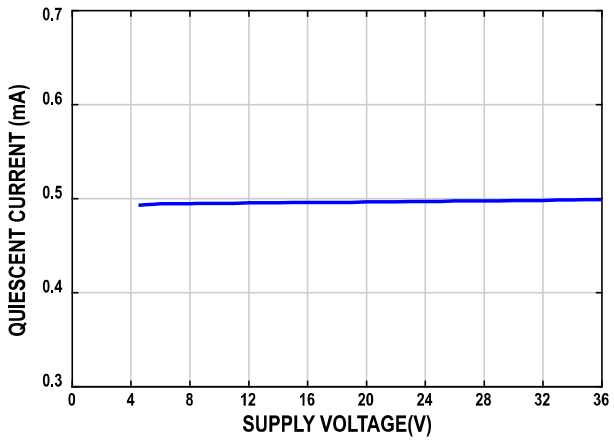

Figure 26. Quiescent Current vs. Supply Voltage

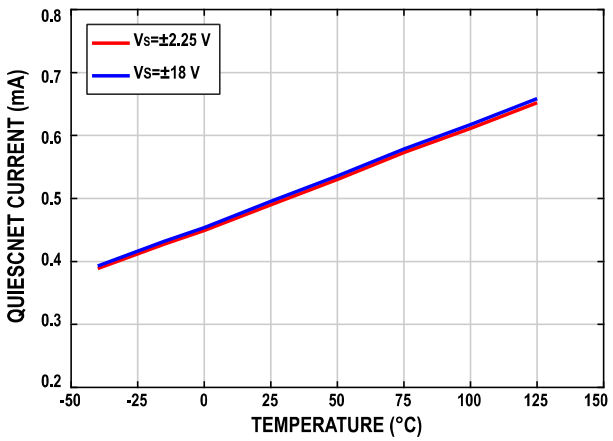

Figure 27. Quiescent Current vs. Temperature

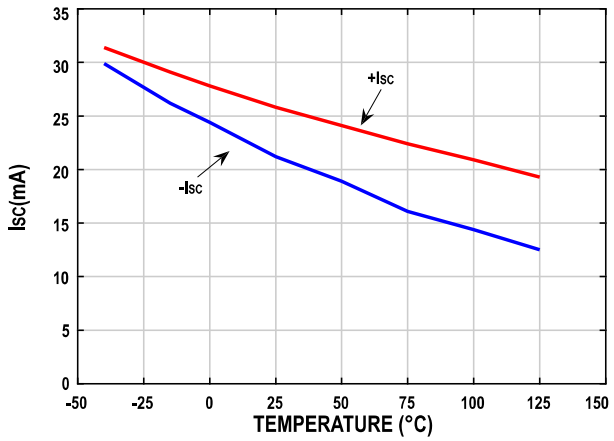

Figure 28. Short-Circuit Current vs. Temperature

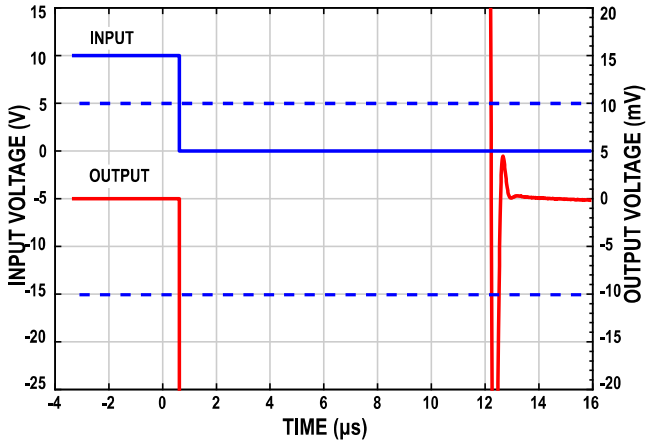

Figure 29. Settling Time

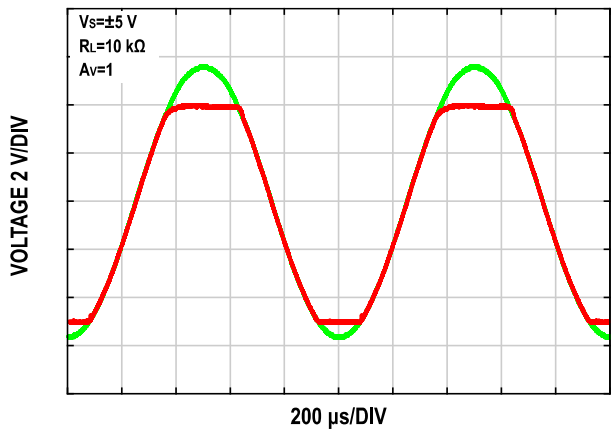

Figure 30. No Phase Reversal

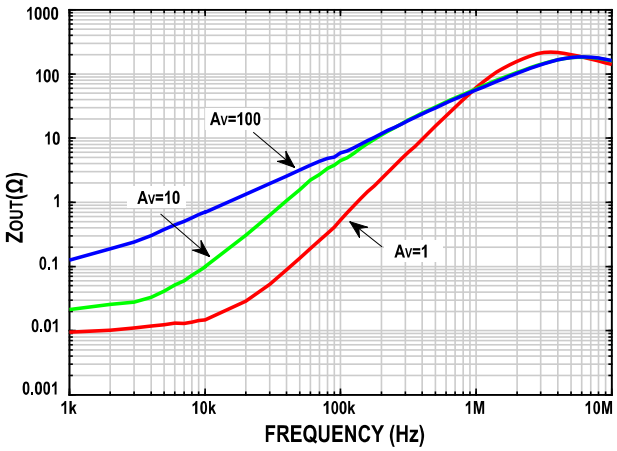

Figure 31. Closed-Loop Output Impedance

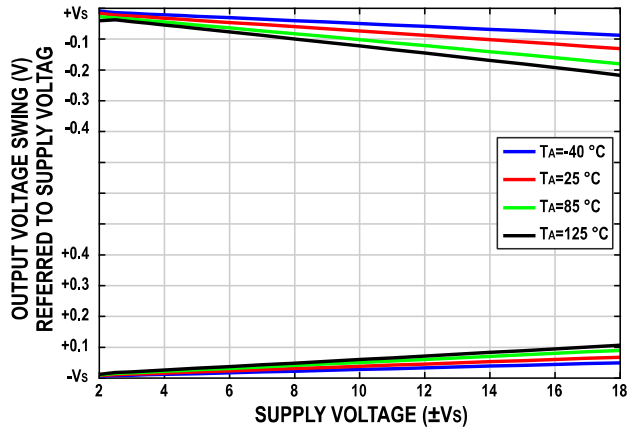

Figure 32. Output Voltage Swing vs. Supply Voltage, R_L=10 kΩ

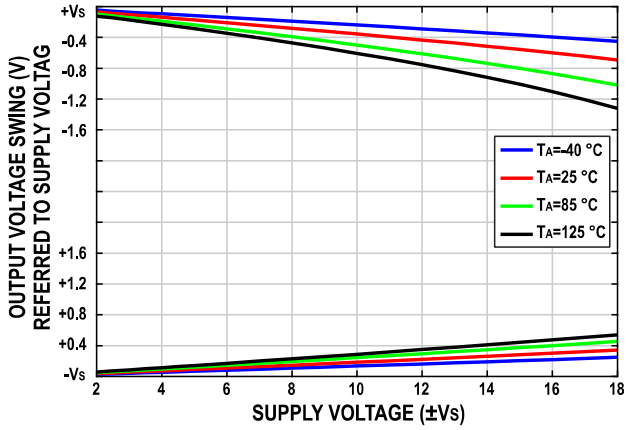

Figure 33. Output Voltage Swing vs. Supply Voltage, R_L=2 kΩ

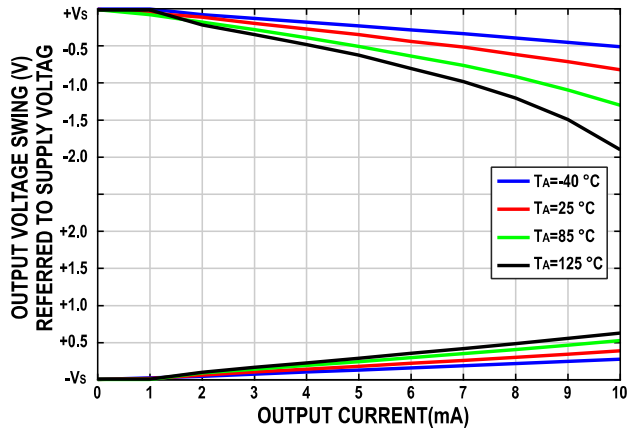

Figure 34. Output Voltage Swing vs. Output Current

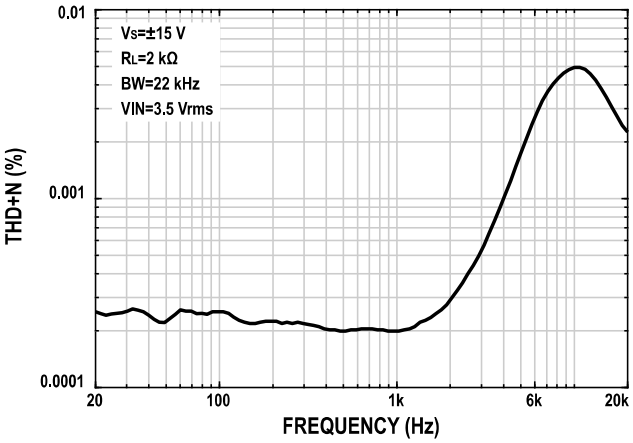

Figure 35. THD+N vs. Frequency

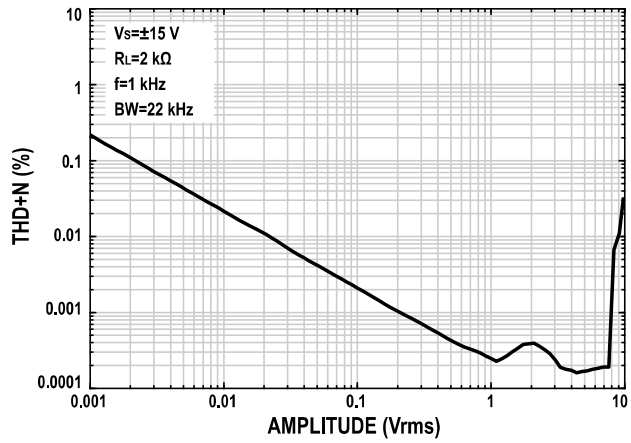

Figure 36. THD+N vs. Amplitude

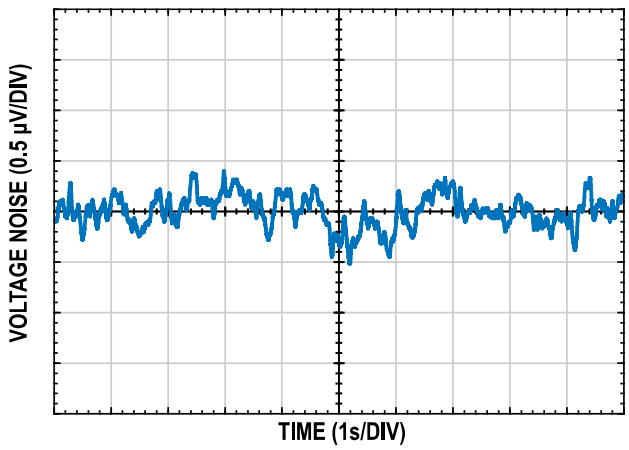

Figure 37. 0.1 Hz to 10 Hz Noise

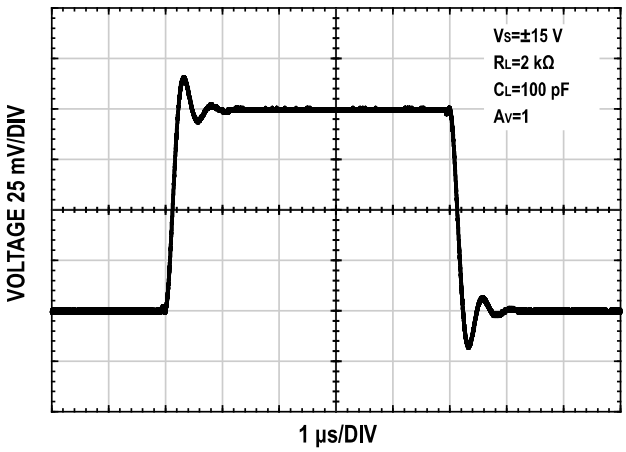

Figure 38. Small Signal Response

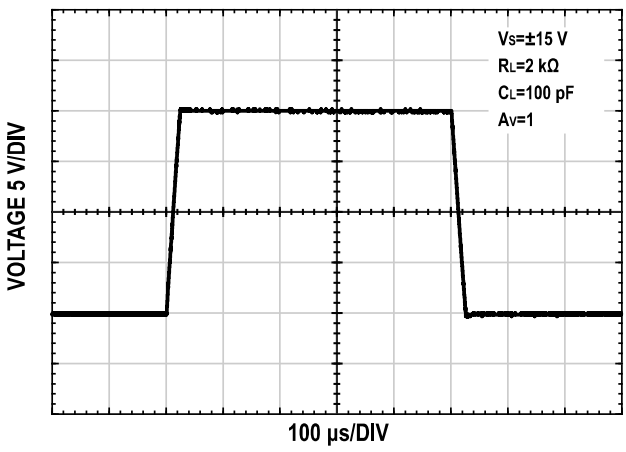

Figure 39. Large Signal Response

Theory of Operation

Post-package Trimming

The ZJA3008 precision operational amplifier boasts a carefully designed MOS input stage, enabling it to maintain an exceptionally low input current of 25 pA maximum at 25 °C. Taking precision to the next level, the ZJA3008 employs ZJW's proprietary post-package trimming technology ZHIJINGTRIM®. This innovative approach involves fine-tuning adjustments (as shown in Figure 40), offering distinct advantages over traditional laser trimming techniques used at the wafer test stage. This post-package trimming method not only minimizes inherent process variations introduced during wafer manufacturing, but also significantly reduces additional defects potentially generated during the plastic molding process. Ultimately, the trimming results in the ZJA3008's exceptional performance: ultra-low offset voltage (10 µV maximum at 25 °C) and ultra-low offset voltage drift (0.5 µV/°C maximum across the specified temperature range in SOIC-8 package). Furthermore, ZJA3008 delivers consistent high accuracy cross wide supply voltage range from 4.5 V to 36 V. These remarkable characteristics make the ZJA3008 the ideal choice for demanding applications, such as high-impedance sensors interface, precision filtering and high-voltage high-precision data acquisition.

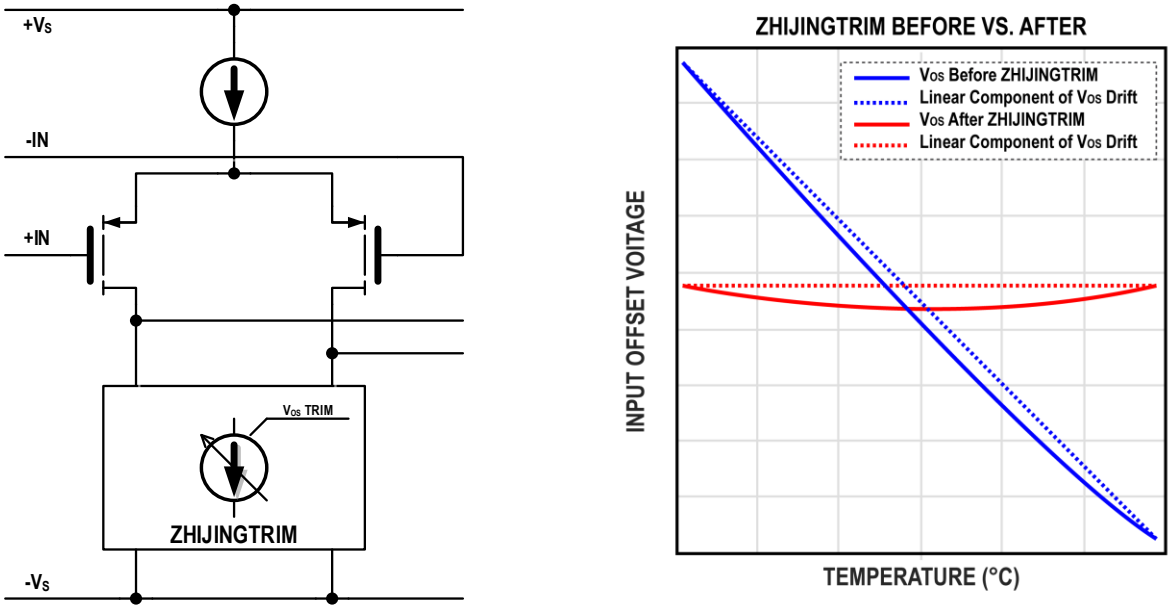

Figure 40. Diagram of Post-package Trimming Scheme (Left) and Effect (Right)

Applications Information

Source Impedance, Input Bias Current Affect both Output Noise and System Offset Voltage

As shown in Figure 41, the output noise density of classic bipolar input stage amplifiers #1, #2, and ZJA3008 is depicted at the 1 kHz frequency point under various source impedances. Bipolar amplifiers typically have large input bias current, leading to significant input current noise. When the source impedance exceeds 100 kΩ, the system noise rapidly increases. In contrast, the ZJA3008 has exceptionally low input bias current, resulting in minimal input noise current, thus its noise contribution to the system is negligible. When the source impedance surpasses 10 kΩ, the system noise is mainly contributed by the source impedance, which appears in the graph as a straight line overlapping the black line representing the noise contributed by source impedance. Similarly, high source impedance can cause considerable system offset voltage and its temperature drift due to the amplifier's input bias current, input offset current, and their temperature drifts. These effects are common in bipolar input amplifiers and zero-drift amplifiers. The ZJA3008, however, leverages its exceptional low input current to fully guarantee low system offset voltage and its temperature drift.

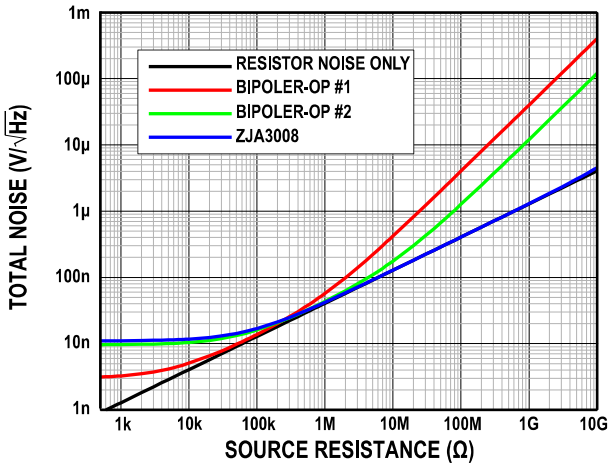

Figure 41. System Total Noise vs. Source Impedance

Input Common Mode Voltage Range

While traditional bipolar amplifiers demand 1 V to 2 V of headroom from both supply rails for proper input common-mode voltage operation, often necessitating dual-supply configurations for applications with 0 V input common-mode signals, the ZJA3008 offers a distinct advantage. It accepts input common-mode voltages down to the negative supply rail, enabling seamless operation with both single and dual power supply designs. As illustrated in Figure 10, this capability, along with its wide supply voltage range (4.5 V to 36 V) and rail-to-rail output, empowers the ZJA3008 to address a broader spectrum of application requirements with exceptional flexibility.

Output Phase Reversal

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ZJA3008 is immune to phase reversal problems even at input voltages beyond the supplies.

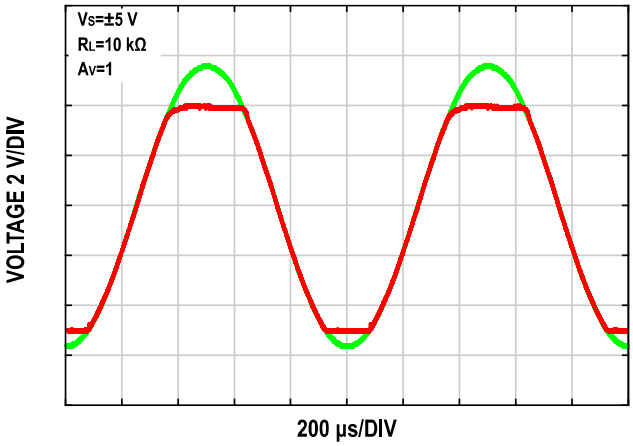

Figure 42. ZJA3008 Has No Output Phase Reversal

Overload Recovery Time

Many zero-drift amplifiers, whether auto-zero or chopping, are plagued by a long overload recovery time, often in ms, due to the complicated settling behavior of the internal nulling loops after saturation of the outputs. Recovery time is important in many applications, particularly where the operational amplifier must amplify small signals in the presence of large transient voltages. The ZJA3008, as a continuous signal processing amplifier, stands out in this regard. Compared to zero-drift amplifiers, its overload recovery time is significantly shorter, falling within a remarkable 2 µs, as demonstrably shown in the table below.

Model	Positive Overload Recovery (µs)	Negative Overload Recovery (µs)
ZJA3008	2	2
Competitor A	12.3	18

Over Temperature Protection

Due to its high operating voltage (up to 36 V) and short-circuit current (up to 25 mA), the ZJA3008 can dissipate up to 1 W of power during use. As thermal resistance for various package formats typically exceeds 100 °C/W, self-heating and the risk of permanent damage from high temperatures are concerns in real-world applications. To address this, the ZJA3008 incorporates an automatic over-temperature protection (OTP) function. When the chip temperature reaches 150 °C, OTP triggers, putting the chip into shutdown mode. Both input and output terminals enter a high-impedance state, significantly reducing power consumption and facilitating temperature drop. Once the chip cools down to 130 °C, OTP disengages, and the chip resumes normal operation.

Input Bias Current Return Path

As shown in Figure 43, a simple AC coupling can be achieved by connecting a capacitor (C_{IN}) in series between the non-inverting input (+) of the operational amplifier and the actual input (VIN) to isolate the DC voltage component of the input voltage. This coupling method is especially common in high-gain applications: when the gain is high, even a small DC voltage component at the amplifier input can affect the available output dynamic range of the op amp, and may even cause output saturation. However, for this AC coupling method located at the high-impedance input, if the input current of the positive input is not provided with a proper bias current return path, it will cause serious bias problems: in fact, the input bias current will slowly charge/discharge the capacitor C_{IN}, depending on the polarity of the input bias current, the capacitor will charge to the positive supply voltage or discharge to the negative supply voltage. This bias current caused offset voltage will be amplified by the op amp's closed-loop DC gain until the op amp's input voltage exceeds its input voltage range or the amplified output voltage exceeds its output voltage range, and this process may take a long time. For example, for an operational amplifier with an FET input stage, if its input current is 1 pA, through a 0.1 μF capacitor, the offset voltage will be ramped at the speed of:

$$10\ pA/0.1\ \mu F=10\ \mu V/s=0.6\ mV/min=36\ mV/h$$

When the closed-loop DC gain is 100, the output voltage ramp rate is 3.6 V/h. Therefore, the actual circuit will not show obvious failure until after several hours. Using an AC coupled oscilloscope for a short-term test may not be able to find this problem.

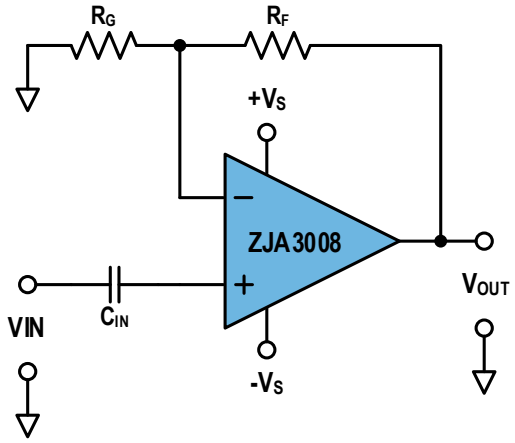

Figure 43. Incorrect AC-Coupled Op Amp Circuit

One simple solution is shown in Figure 44. A resistor (R_{IN}) is connected between the input of the operational amplifier and ground, providing an input bias current return path. Unlike operational amplifiers with FET inputs, traditional bipolar operational amplifiers need to set R_{IN} to the parallel value of R_G and R_F to minimize the input offset voltage caused by input bias current, considering the mis-matching between the two inputs of the op amp. Since this resistor will introduce additional noise to the overall circuit, the value of the input coupling capacitor and the resistor should be balanced between non-ideal factors such as input impedance, input high-pass cutoff frequency, and input offset voltage according to actual needs. Typical resistor value is generally between 100 kΩ and 1 MΩ.

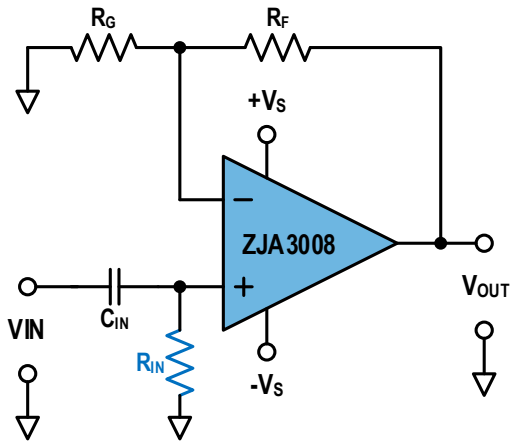

Figure 44. Creating an Input Bias Current Return Path

Temperature Hysteresis

Temperature hysteresis, that is, the stability vs. cycling of temperature. Hysteresis is an important parameter because it tells the system designer how closely the signal returns to its starting amplitude after the ambient temperature changes and subsequent return to room temperature. Figure 45 shows the change in input offset voltage as the temperature cycles three times from room temperature to 125 °C to −40 °C and back to room temperature. In the three full cycles, the offset hysteresis is within 2 µV, compared with the competitor A's data shown in Figure 46, it is significantly better without precondition, which is required for competitor A.

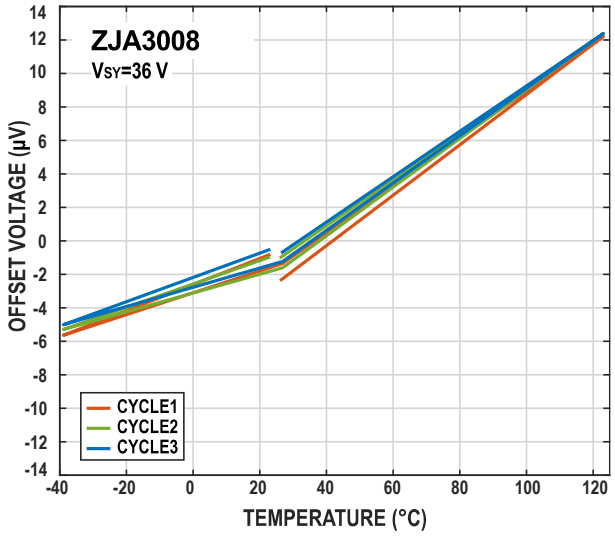

Figure 45. ZJA3008 Offset Voltage over Three Full Temperature Cycles

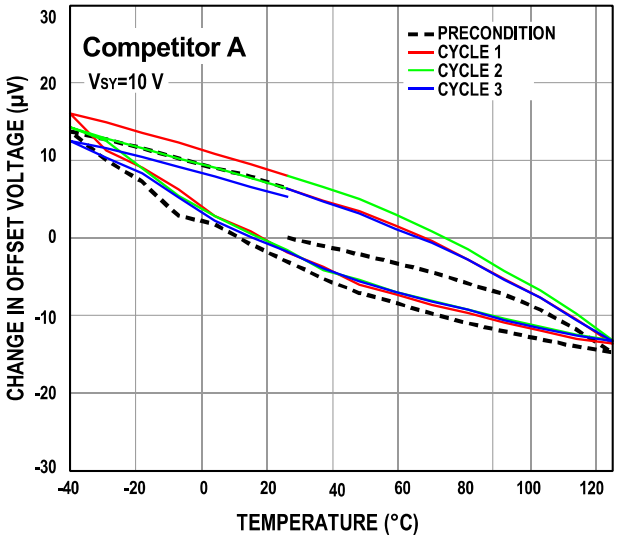

Figure 46. Competitor A Offset Voltage over Three Full Temperature Cycles

The histogram in Figure 47 shows that ZJA3008's hysteresis is similar no matter the device is cycled through full or only a half cycle, from room temperature to 125 °C and back to room temperature. In contrast, Competitor A's hysteresis demonstrates significant difference between full cycle and half cycle.

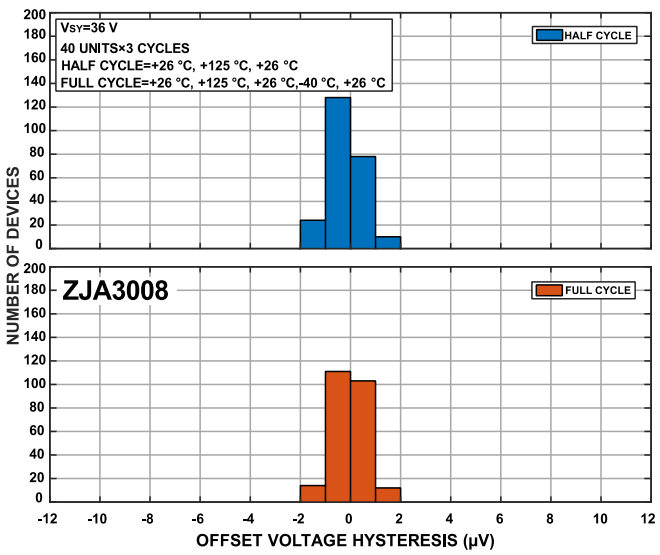

Figure 47. Histogram Showing the ZJA3008's Temperature Hysteresis of the Offset Voltage over Three Full Cycles and over Three Half Cycles

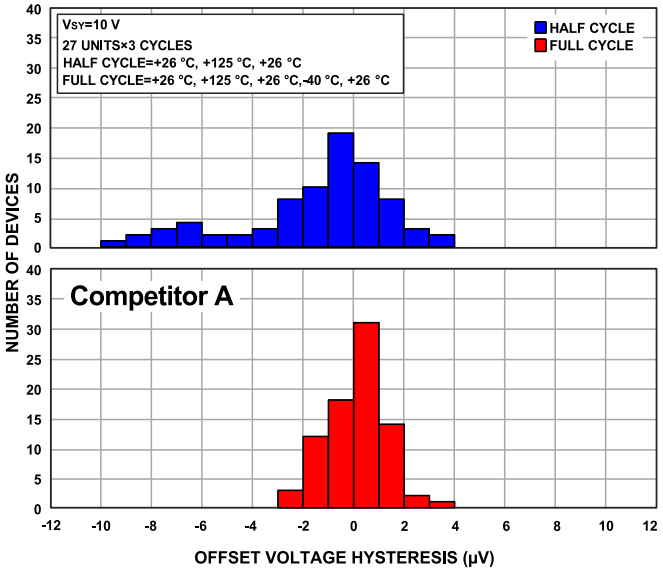

Figure 48. Histogram Showing the Competitor A's Temperature Hysteresis of the Offset Voltage over Three Full Cycles and over Three Half Cycles

ZJA3008 exhibits significantly smaller and more consistent temperature hysteresis, regardless of whether it's cycled through a full or half cycle. This makes it more suitable for precision signal conditioning to build more reliable systems. What's more, ZJA3008 does not require the precondition process that is necessary for competitor A. This feature makes it is very easy of use with high performance and can lower the system cost.

Applications and Implementation

Bandpass KRC Filter

The ZJA3008 series of amplifiers are particularly suitable for use in the design of precision filters, such as the typical KRC filter, as shown in Figure 49. With their excellent low offset and high CMRR performance, precision filters using ZJA3008 can guarantee stable performance over a wide input range while also having sufficient output dynamic range even at high gain. On the other hand, due to the ZJA3008-2 and ZJA3008-4's ultra-high channel separation, even using the dual amplifiers in the same ZJA3008-2 can achieve excellent filter design without worrying about performance degradation caused by channel crosstalk.

ZJA3008's power supply current of 500 μA makes it suitable for both portable, battery powered systems and line powered systems.

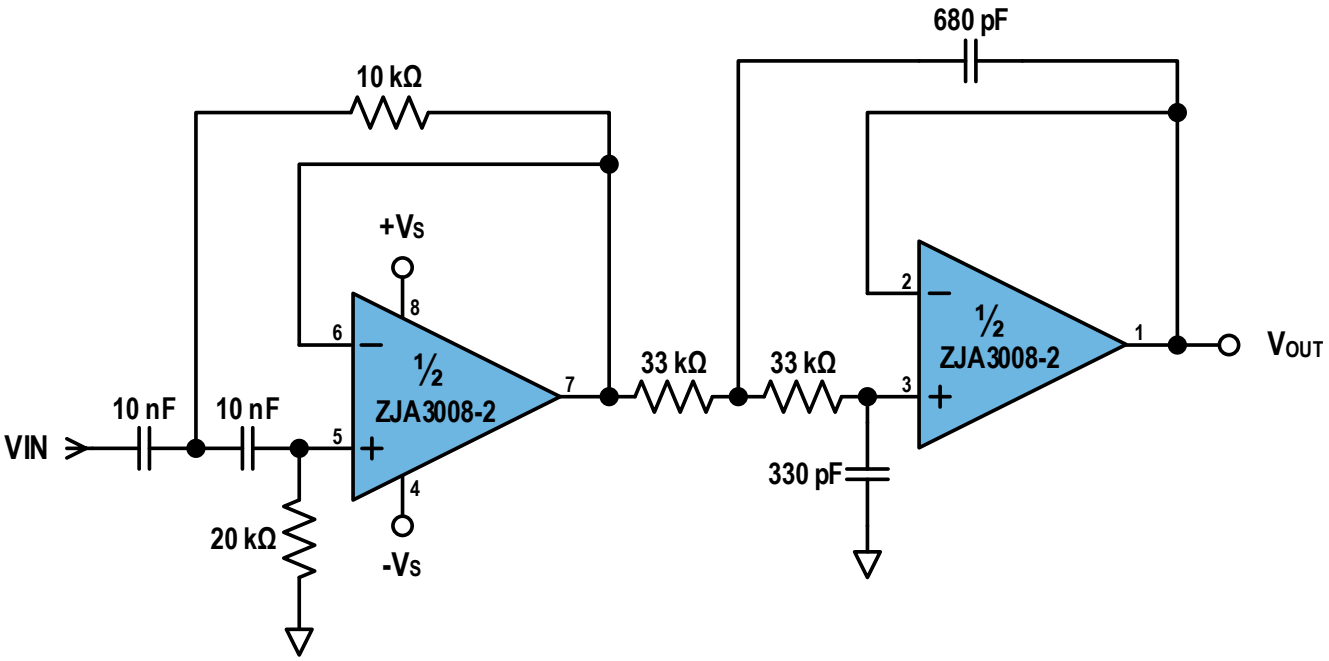

Figure 49. Using ZJA3008-2 to Build a 2-stage Band-pass KRC Filter

Layout Guidance

For optimized performances of the device, good PCB layout practices are recommended, including:

- Noise may be conducted into the analog circuit through the op amp supply pins, using the low ESR 0.1 μF ceramic capacitor as decoupling capacitor. Put it as close as possible to the power pin can effectively reduce the noise caused by the power supplies.
- Normally input trace is more sensitive, keep the trace as short as possible. In order to reduce the noise of parasitic coupling, keep the input signals far from the power supply and/or outputs. If this is not possible, the sensitive traces should be perpendicular to others, so that the noise coupled through the parasitic capacitance can be as small as possible.
- If the it is high impedance signal source, it is necessary to design a guard ring. Guard rings can significantly reduce leakage currents from nearby traces that are at different potentials.
- Place the peripheral components as close as possible to the pins of the op amp, such as placing R_F, C_F and R_G. And delete the PCB ground plane below the inverting input to minimize parasitic capacitance.
- For best leakage performance, it is recommended to clean the PCBA after soldering and baking at 85 °C for 30 minutes to remove any potential moisture from the package.
- In addition, separate grounding of the analog and digital parts of the circuit is one of the simplest and most effective noise suppression methods. When designing the PCB, plan the layout of the ground current return paths of the analog and digital parts so that the ground current return paths do not interfere each other. Using one or more layers of the multi-layer PCB as the ground also helps to reduce the ground impedance and noise.

Outline Dimensions

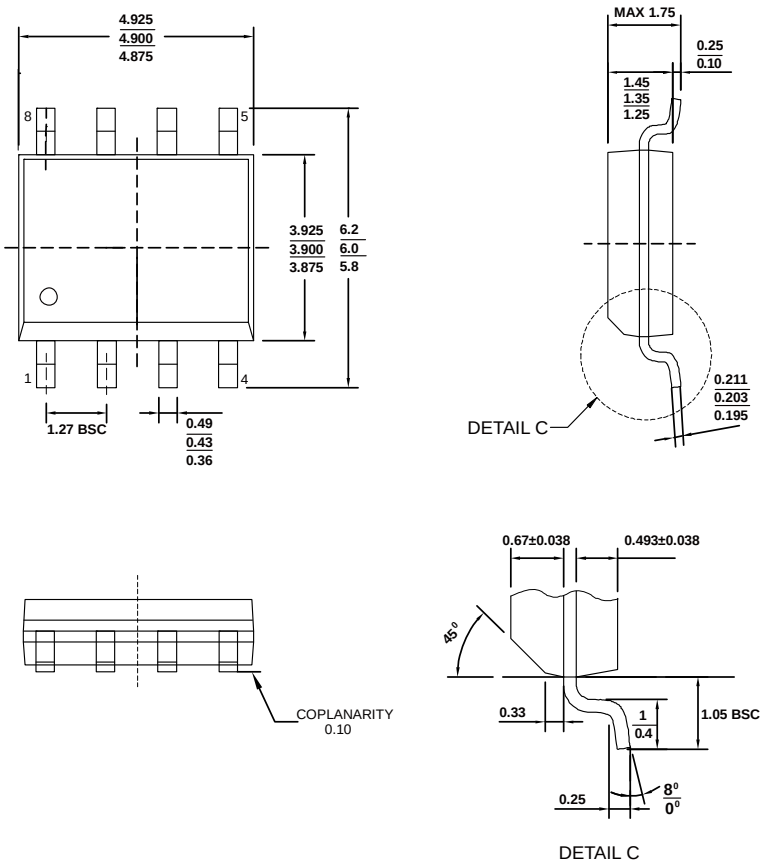

Figure 50. 8-Lead SOIC Package Dimensions shown in millimeters

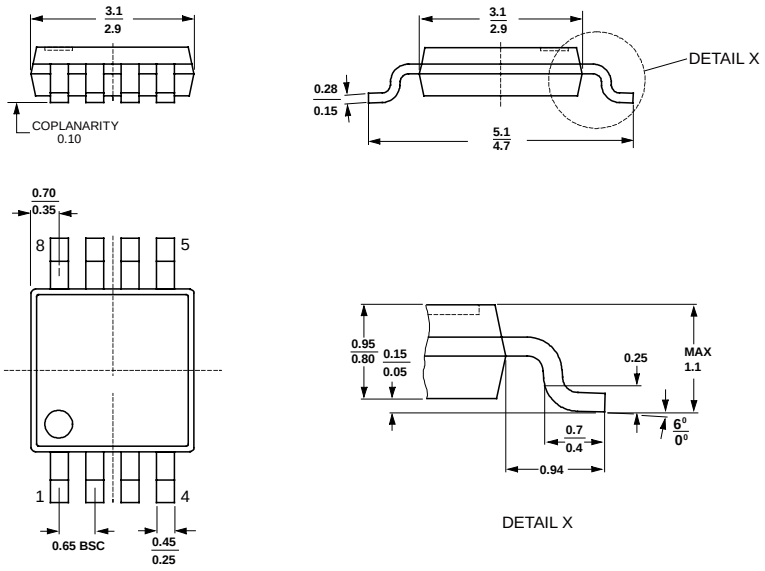

Figure 51. 8-Lead MSOP Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Status[1]	Package	Maximum V_{OS}&TCV_{OS}	Temperature Range (°C)	External Package
ZJA3008-2	ZJA3008-2BSABT	ACTIVE	SOIC-8	10 μV & 0.5 μV/°C	-40 to 125	Tube
	ZJA3008-2BSABR					13" reel
	ZJA3008-2ASABT	ACTIVE	SOIC-8	20 μV & 1.0 μV/°C	-40 to 125	Tube
	ZJA3008-2ASABR					13" reel
	ZJA3008-2BUABT	ACTIVE	MSOP-8	10 μV & 0.5 μV/°C	-40 to 125	Tube
	ZJA3008-2BUABR					13" reel
	ZJA3008-2AUABT	ACTIVE	MSOP-8	20 μV & 1.0 μV/°C	-40 to 125	Tube
	ZJA3008-2AUABR					13" reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T=tube; R=reel
- Temperature range: A= -40 °C to 125 °C Automotive Grade 1; B= -40 °C to 125 °C; E= -40 °C to 85 °C
- Number of Pins: K=5; T=6, A=8; B=10; D=14; E=16; P=20;
- Package type: S=SOIC; U=MSOP, TSSOP, SOT; T=DFN, QFN
- Grade: B grade is better than A grade
- Base: R=Voltage reference; A=Amplifier; C=Data Converter; G=Switch and Multiplexer; M=Others

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may be available.
OBSOLETE: ZJW has discontinued the production of the device.

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1nV-S glitch, MSOP-10/8, SOIC-8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, input to V-, RRO, 4.5 V to 36 V
ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, RRO, 4.5 V to 36 V
ZJA3512-2	Dual/Quad 36 V 7MHz precision JFET Op Amps	7 MHz GBW, 35 V/µS SR, 50 µV max Vos, 1 µV/°C max Vos drift, 2 mA/Amplifier, RRO, 9 V to 36 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G=1), 25 pA max Ibias, 25 µV max Vosi, gain error 1 ppm max (G=1), 3.3 mA Iq, ±2.4 V to ±18 V, -40 ºC to 125 ºC specified
ZJA3622/8	36 V low-cost precision in-amp	CMRR 93 dB min (G=10), 0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G=10), 3.3 mA Iq, ±2.4 V to ±18 V
ZJA3611, ZJA3609	36 V ultra-high precision wider bandwidth precision in-amp (min gain of 10)	CMRR 120 dB min (G=10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G=10), 3.3 mA Iq, ±2.4 V to ±18 V, -40 ºC to 125 ºC specified
ZJA3676/7	Low power, G=1 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min, Vos 100 µV max, gain error 15 ppm max, 500 kHz BW, 330 µA/channel, 2.7 V to 36V
ZJA3100	15 V precision fully differential amplifier	145 MHz GBW, 447 V/µS SR, 16-bit settling time 50 nS, 50 µV max Vos, 4.6 mA Iq, 3 V to 15 V, SOIC/MSOP-8, QFN-16
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT}=2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 ºC to 125 ºC
ZJR1000	15 V supply precision voltage reference	V_{OUT}=1.25/2.048/2.5/3/4.096/5 V, 5 ppm/°C max drift -40 ºC to 125 ºC
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT}=2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 ºC to 125 ºC, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MS-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection up to ±50 V power on & off, latch-up immune, Ron 270 Ω,14.8 pC charge injection, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω,14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch<100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV