

## 36 V Precision, Low Bias Current Op Amps

### Features

- Low Offset Voltage:
  - 35  $\mu\text{V}$  max (SOIC package)
  - 55  $\mu\text{V}$  max (other packages)
- Low Offset Voltage Temperature Drift:
  - 0.5  $\mu\text{V}/^\circ\text{C}$  max (B Grade, SOIC package)
  - 1.0  $\mu\text{V}/^\circ\text{C}$  max (A Grade, SOIC package)
- Low Input Bias Current: 25 pA max
- Low Noise: 11 nV/ $\sqrt{\text{Hz}}$  ( $f = 1$  kHz)
- CMRR: 120 dB min
- PSRR: 120 dB min (full temperature range)
- $A_{\text{vol}}$ : 120 dB min (full temperature range)
- Supply Current: 1 mA/amplifier
- Gain Bandwidth Product: 3 MHz, unit gain stable
- Single/dual Power Supply:  $\pm 2.25$  V to  $\pm 18$  V, 4.5 V to 36 V
- Specified Temperature Range:  $-40$   $^\circ\text{C}$  to  $+125$   $^\circ\text{C}$

### Applications

- Precision Data Acquisition
- Instrumentation
- Sensor Signal Conditioning
- Industrial Control
- Communication Systems
- Smart Grid

### General Description

ZJA3001 series high-precision continuous operational amplifiers featuring lower than 35  $\mu\text{V}$  offset voltage, better than 0.5  $\mu\text{V}/^\circ\text{C}$  offset voltage drift, 25 pA input bias current and 11 nV/ $\sqrt{\text{Hz}}$  low noise. These features make them exceptionally suitable for precision signal conditioning, such as precision sensor interface, voltage amplification, current to voltage conversion and filtering. ZJA3001 has single, dual and quad channel versions.

The ZJA3001 has a wide power supply voltage range, operating from  $\pm 2.25$  V to  $\pm 18$  V for dual-supply operation or 4.5 V to 36 V for single-supply. It further expands its input capabilities to negative rail, making it ideal for a variety of applications.

Ideal for demanding applications requiring precision and reliability, the ZJA3001 series boast the highest moisture sensitivity level (MSL-1), making them ideal for reflow soldering and high-volume production. They also operate reliably across a wide temperature range of  $-40$   $^\circ\text{C}$  to  $+125$   $^\circ\text{C}$ , making them perfect for precision sensor interfaces, medical instrumentation, and industrial control systems.

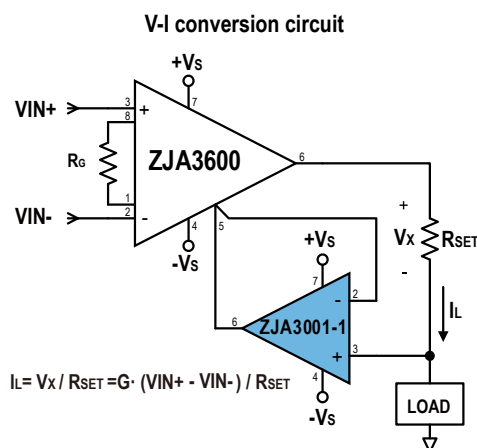
ZJA3001 series are available in single, dual, and quad configurations:

ZJA3001-1 (single): SOIC-8 and MSOP-8

ZJA3001-2 (dual): SOIC-8 and MSOP-8

ZJA3001-4 (quad): SOIC-14 and TSSOP-14

### Application Examples



### Typical Performance Characteristics

25  $^\circ\text{C}$  Offset Voltage Distribution, SOIC-8 Package

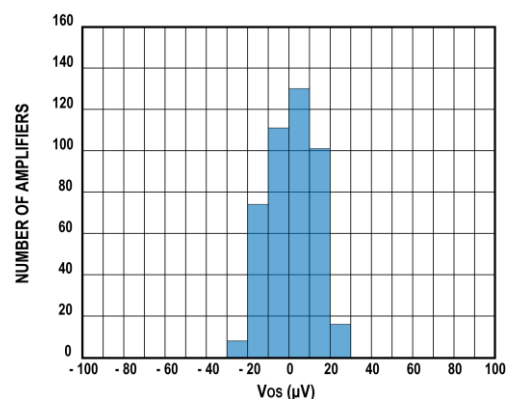


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## Version (Release B ) <sup>1</sup>

### Revision History

#### **Nov 2024**—**Release B**

Updated Pin Configurations, Outline Dimensions, Ordering Guide, Orderable Device Explanation, Related Parts

#### **April 2024**

Updated Feature, Orderable Device Explanation

#### **June 2023**—**Release A**

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Pin Configurations and Function Descriptions

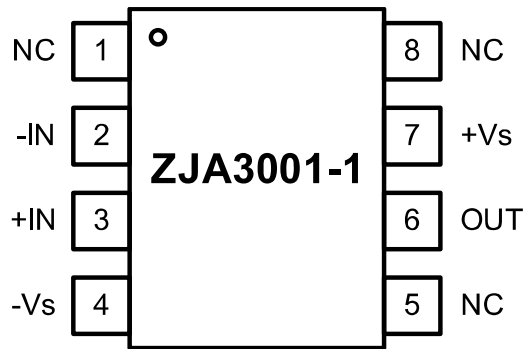


Figure 1. ZJA3001-1 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O <sup>1</sup>	Description
NC	1, 5, 8	--	No internal circuit connection
-IN	2	AI	Inverting input
+IN	3	AI	Non-inverting input
-Vs	4	--	Negative power supply
OUT	6	AO	Output
+Vs	7	--	Positive power supply

<sup>1</sup> AI: Analog Input; P: Power; AO: Analog Output.

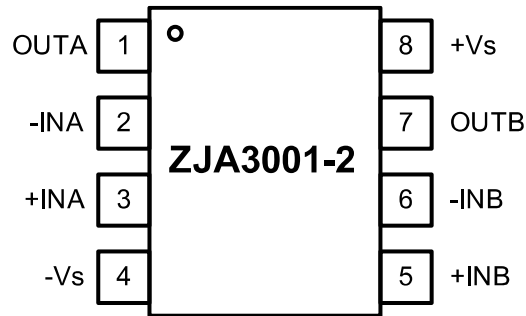


Figure 2. ZJA3001-2 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O <sup>1</sup>	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
-Vs	4	--	Negative power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
+Vs	8	--	Positive power supply

<sup>1</sup> AI: Analog Input; P: Power; AO: Analog Output.

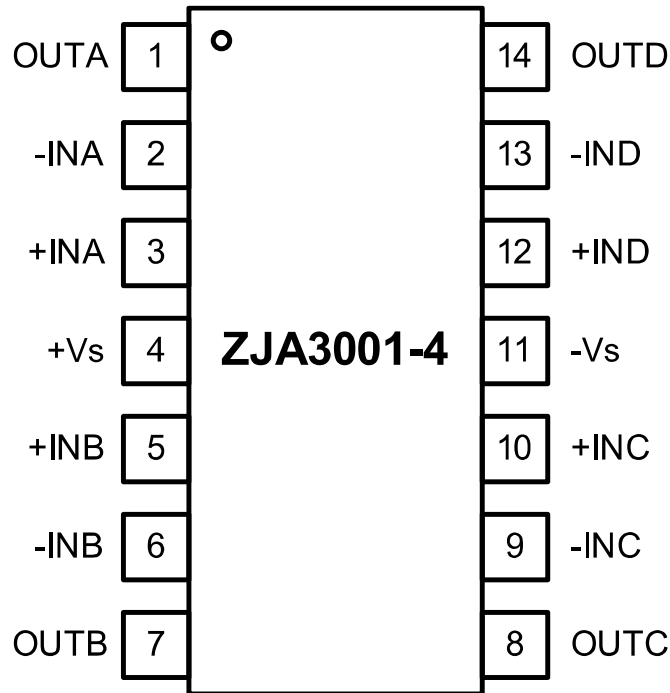


Figure 3. ZJA3001-4 Pin Configuration (14-lead SOIC and TSSOP)

Mnemonic	Pin No.	I/O <sup>1</sup>	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
+Vs	4	--	Positive power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
OUTC	8	AO	Channel C output
-INC	9	AI	Channel C inverting input
+INC	10	AI	Channel C non-inverting input
-Vs	11	--	Negative power supply
+IND	12	AI	Channel D non-inverting input
-IND	13	AI	Channel D inverting input
OUTD	14	AO	Channel D output

<sup>1</sup> AI: Analog Input; P: Power; AO: Analog Output.

Absolute Maximum Ratings <sup>1</sup>

Parameter	Rating
Supply Voltage	40 V
Input Voltage	$\pm V_{SY}$
Input Current <sup>2</sup>	$\pm 10$ mA
Differential Input Voltage	$(+V_{SY}) - (-V_{SY})$
Output Short-Circuit Duration to GND <sup>3</sup>	Continuous
Operating Temperature Range	-40 °C to +125 °C
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature Range	-65 °C to +150 °C
Maximum Reflow Temperature <sup>4</sup>	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
Electrostatic Discharge (ESD) <sup>5</sup>	
Human Body Model (HBM) <sup>6</sup>	1.5 kV
Charged Device Model (CDM) <sup>7</sup>	1 kV

Thermal Resistance <sup>8</sup>

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
SOIC-8	158	43	°C/W
SOIC-14	120	36	°C/W
MSOP-8	190	44	°C/W
TSSOP-14	240	43	°C/W

<sup>1</sup> These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup> There are clamping diodes between the input pins and the power pins, and also between each other. When the input signal exceeds the supply rail by 0.3 V, the input current is limited to 10 mA.

<sup>3</sup> Limited by Over Temperature Protection (OTP).

<sup>4</sup> IPC/JEDEC J-STD-020 Compliant

<sup>5</sup> Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

<sup>6</sup> ANSI/ESDA/JEDEC JS-001 Compliant

<sup>7</sup> ANSI/ESDA/JEDEC JS-002 Compliant

<sup>8</sup>  $\theta_{JA}$  addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

## Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at  $V_S = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	B Grade, SOIC-8/SOIC-14	●	15 25	35 65	$\mu\text{V}$ $\mu\text{V}$
		A Grade, SOIC-8/SOIC-14	●	15 40	35 100	$\mu\text{V}$ $\mu\text{V}$
		B Grade, MSOP-8/TSSOP-14	●	25 40	55 85	$\mu\text{V}$ $\mu\text{V}$
		A Grade, MSOP-8/TSSOP-14	●	25 70	55 160	$\mu\text{V}$ $\mu\text{V}$
Offset Voltage Drift	$TCV_{OS}$	B Grade, SOIC-8/SOIC-14	●	0.25	0.5	$\mu\text{V}/^\circ\text{C}$
		A Grade, SOIC-8/SOIC-14	●	0.5	1.0	$\mu\text{V}/^\circ\text{C}$
		B Grade, MSOP-8/TSSOP-14	●	0.4	0.8	$\mu\text{V}/^\circ\text{C}$
		A Grade, MSOP-8/TSSOP-14	●	0.7	1.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$		●	5	25	$\mu\text{A}$ $\text{nA}$
Input Offset Current	$I_{OS}$		●		10	$\mu\text{A}$ $\text{nA}$
Input Voltage Range	IVR			-13	13	V
Common-ode Rejection Ratio	CMRR	$V_{CM} = -13\text{ V to } 13\text{ V}$	●	120	130	$\text{dB}$
				114		$\text{dB}$
Open-Loop Voltage Gain	$A_{VOL}$	$R_L = 10\text{ k}\Omega$ , $V_o = \pm 10\text{ V}$	●	126	140	$\text{dB}$ $\text{dB}$
		$R_L = 2\text{ k}\Omega$ , $V_o = \pm 10\text{ V}$	●	126	140	$\text{dB}$ $\text{dB}$
Input Resistance/Capacitance	$R_{IN}/C_{IN}$	Differential Mode			1.5/5.7	$\text{G}\Omega/\text{pF}$
		Common Mode			2.5/1.7	$\text{T}\Omega/\text{pF}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage (High)	$V_{OH}$	$R_L = 10\text{ k}\Omega$	●	50 75	150 250	$\text{mV}$ $\text{mV}$
		$R_L = 2\text{ k}\Omega$	●	200 300	350 550	$\text{mV}$ $\text{mV}$
Output Voltage (Low)	$V_{OL}$	$R_L = 10\text{ k}\Omega$	●	40 60	150 250	$\text{mV}$ $\text{mV}$
		$R_L = 2\text{ k}\Omega$	●	160 240	350 550	$\text{mV}$ $\text{mV}$
Short-Circuit Current	$I_{SC}$			67		$\text{mA}$
Open-Loop Output Impedance	$Z_{OUT}$	$F = 1\text{ kHz}$			15	$\Omega$



Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>						
Supply Current (per Amplifier)	$I_{SY}$	$V_O = 0\text{ V}$	•	1.0	1.1 1.2	mA mA
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 3\text{ V to } \pm 18\text{ V}$	•	126 120	140	dB dB
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		2.3		V/ $\mu$ s
Gain Bandwidth Product	GBP	$R_L = 2\text{ k}\Omega, G = 100, V_{IN} = 100\text{ mV}_{P-P}$		3		MHz
Settling Time	$t_s$	to 0.1 %, $G = -1, 0\text{ to } 10\text{ V step}$		4.6		$\mu$ s
		to 0.01 %, $G = -1, 0\text{ to } 10\text{ V step}$		8.8		$\mu$ s
Overload Recovery Time	$t_{OR}$	$R_L = 10\text{ k}\Omega, G = -10, V_{IN} = \pm 2\text{ V step}$		330		ns
Total Harmonic Distortion + Noise	THD+N	$R_L = 2\text{ k}\Omega, G = 1, f = 1\text{ kHz}, V_O = 3.5\text{ V}_{rms}$		-124		dB
Phase Margin	PM	$R_L = 2\text{ k}\Omega, G = 1, V_{IN} = 100\text{ mV}_{P-P}$		55		°
Multiple Amplifier Channel Separation	$C_S$	$R_L = 10\text{ k}\Omega, f = 1\text{ kHz}$		150		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n, P-P}$	0.1 Hz to 10 Hz		2		$\mu$ V $_{P-P}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		11		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		2		fA/ $\sqrt{\text{Hz}}$
<b>OVER TEMPERATURE PROTECTION</b>						
Trigger Temperature	$T_{IN}$			150		°C
Exit Temperature	$T_{EXIT}$			130		°C
<b>TEMPERATURE RANGE</b>						
Specified Temperature Range				-40	125	°C

Typical Performance Characteristics

Unless otherwise stated,  $V_{SY} = \pm 15.0\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .

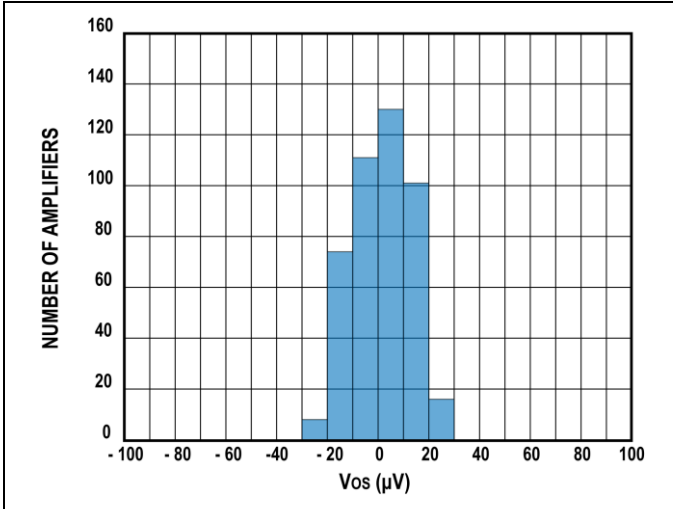


Figure 4. Input Offset Voltage Distribution, SOIC-8 Package

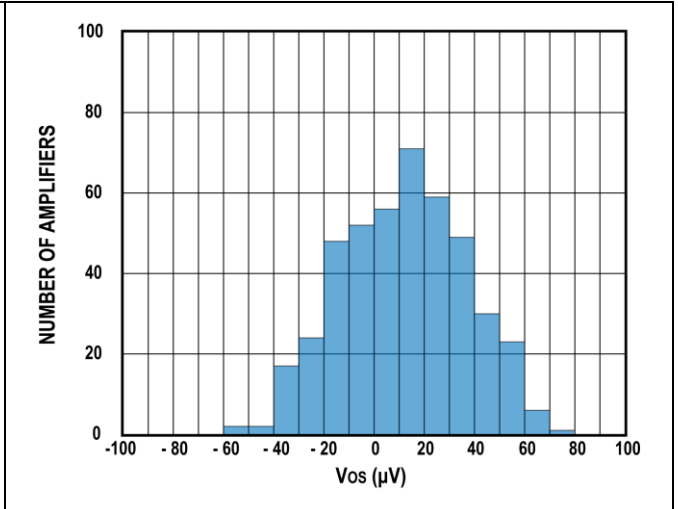


Figure 5. Input Offset Voltage Distribution at -40 °C, SOIC-8 Package

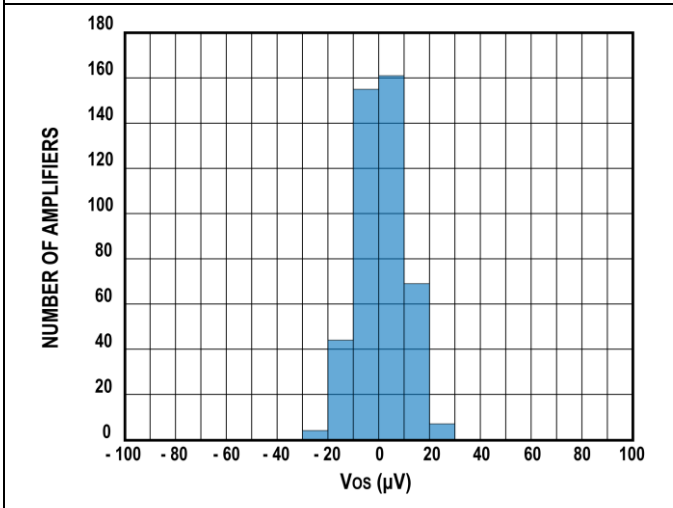


Figure 6. Input Offset Voltage Distribution at 85 °C, SOIC-8 Package

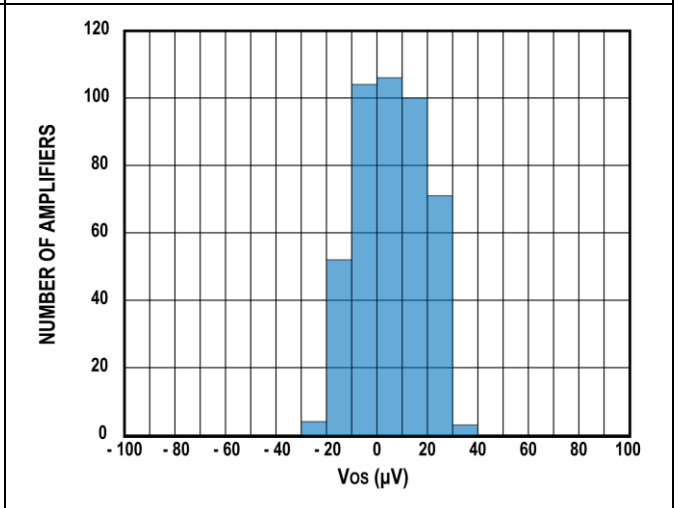


Figure 7. Input Offset Voltage Distribution at 125 °C, SOIC-8 Package

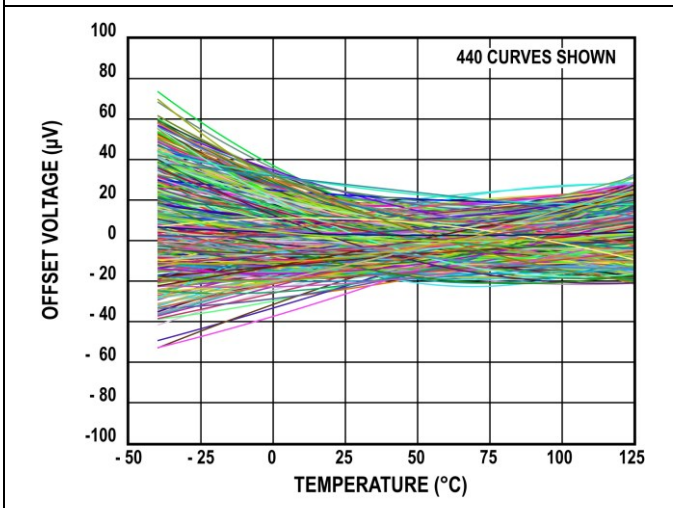


Figure 8. Input Offset Voltage vs. Temperature, SOIC-8 Package

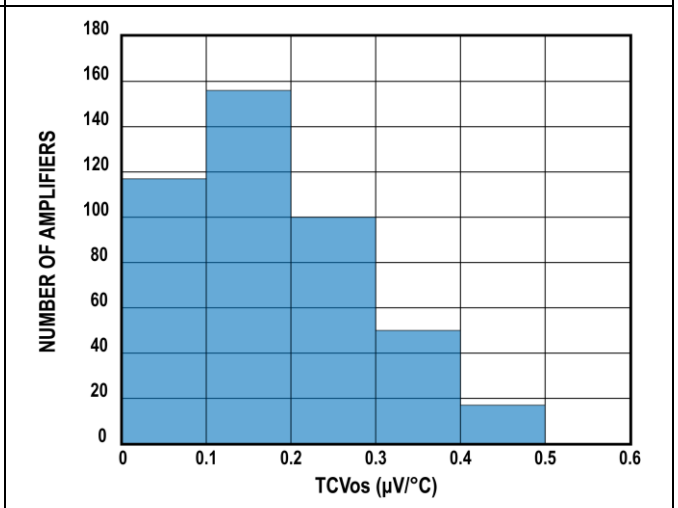


Figure 9. Input Offset Voltage Drift Distribution, SOIC-8 Package

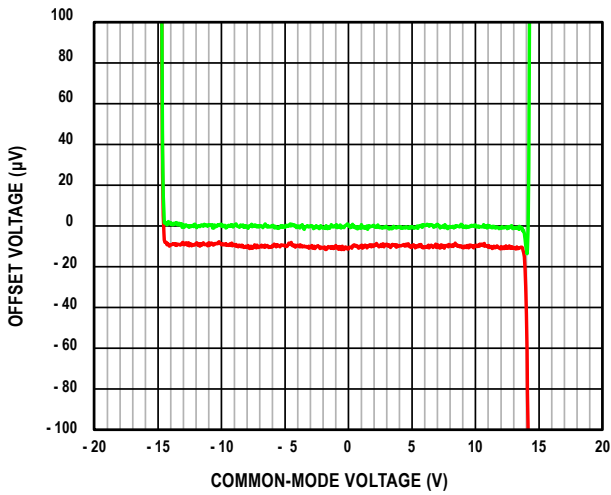


Figure 10. Offset Voltage vs. Input Common-Mode Voltage

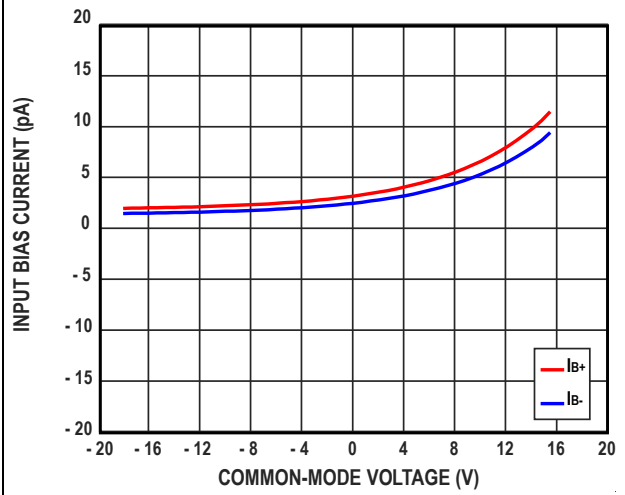


Figure 11. Input Current vs. Input Common-Mode Voltage ( $V_{SY} = \pm 18V$ )

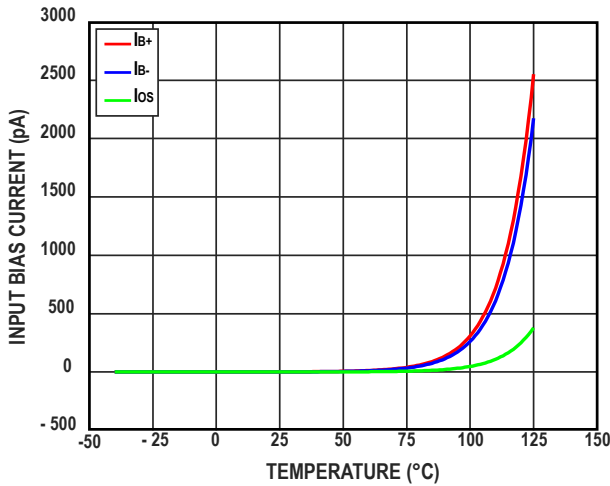


Figure 12. Input Bias Current vs. Temperature

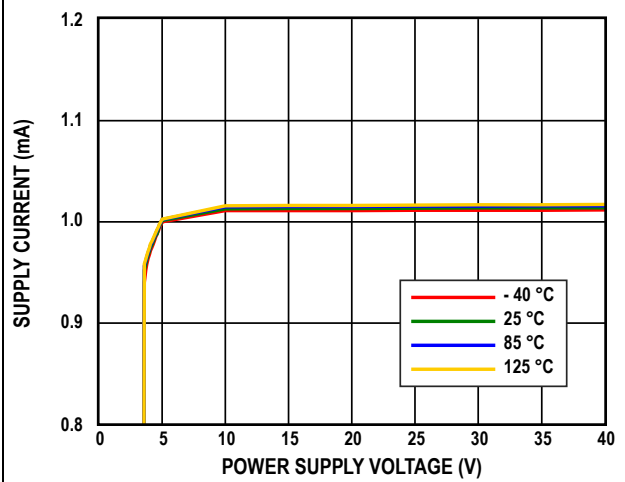


Figure 13. Supply Current per Amplifier vs. Power Supply Voltage

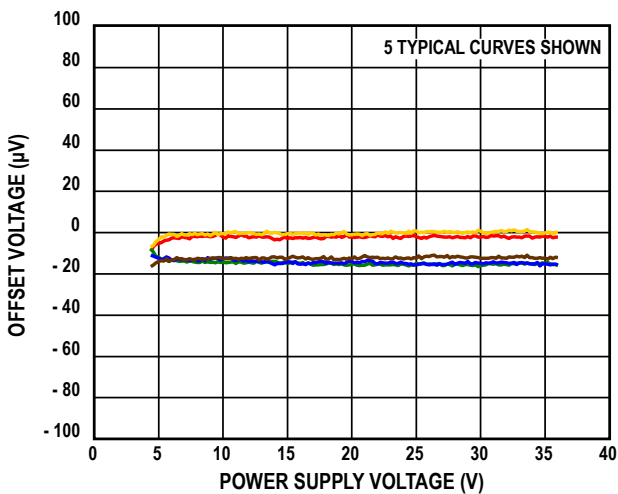


Figure 14. Input Offset Voltage vs. Power Supply Voltage

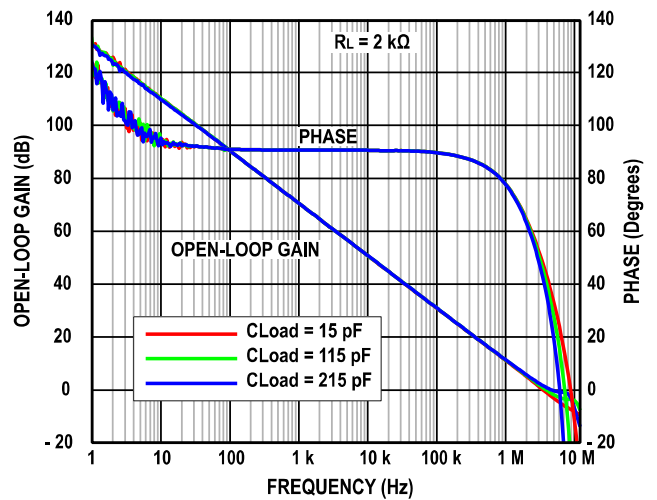


Figure 15. Open-Loop Gain and Phase vs. Frequency

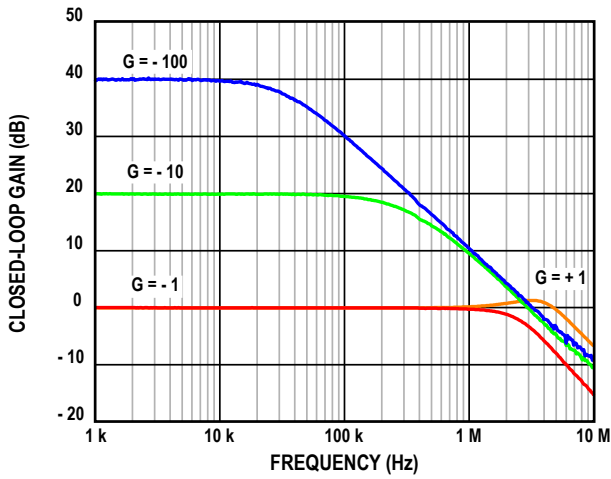


Figure 16. Closed-Loop Gain vs. Frequency

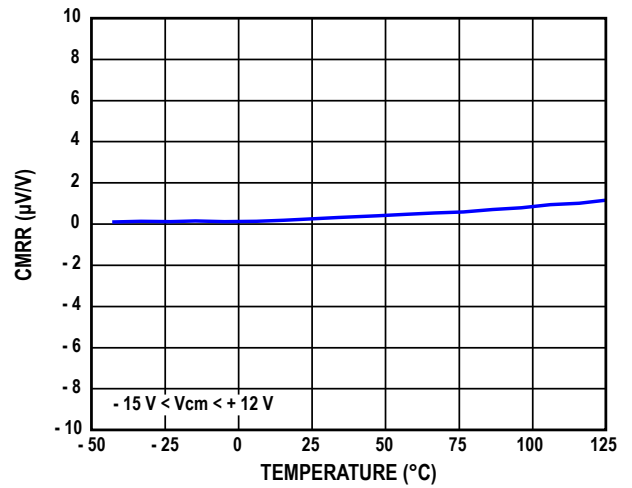


Figure 17. Common Mode Rejection Ratio (CMRR) vs. Temperature

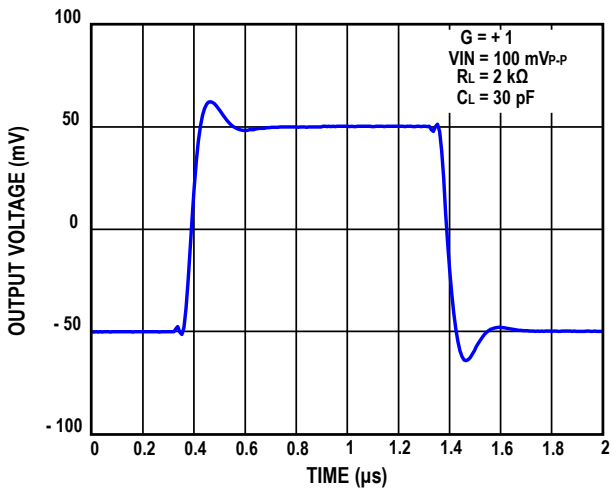


Figure 18. Small Signal Transient Response

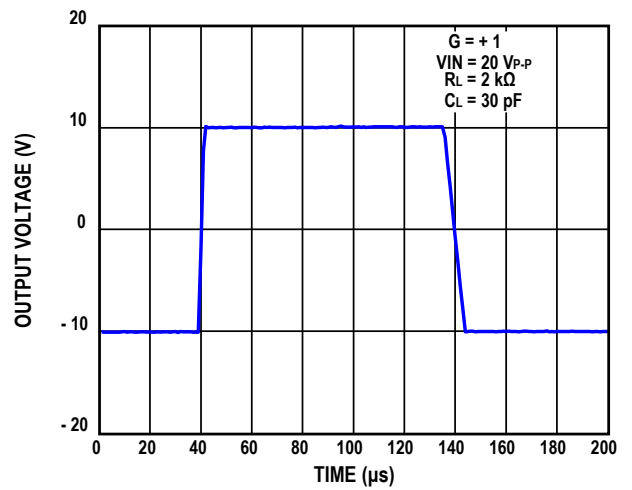


Figure 19. Large Signal Transient Response

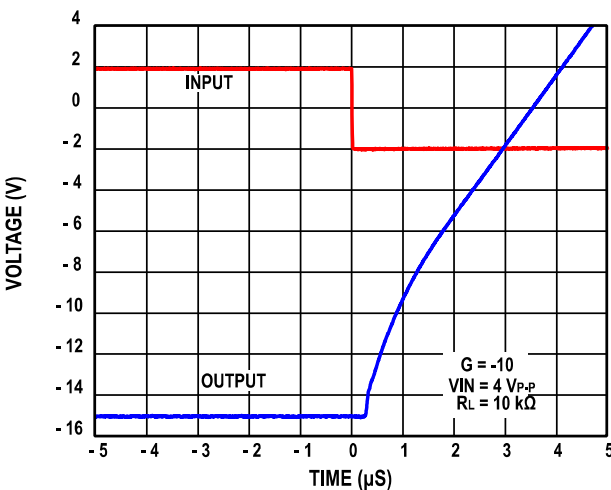


Figure 20. Positive Overload Recovery

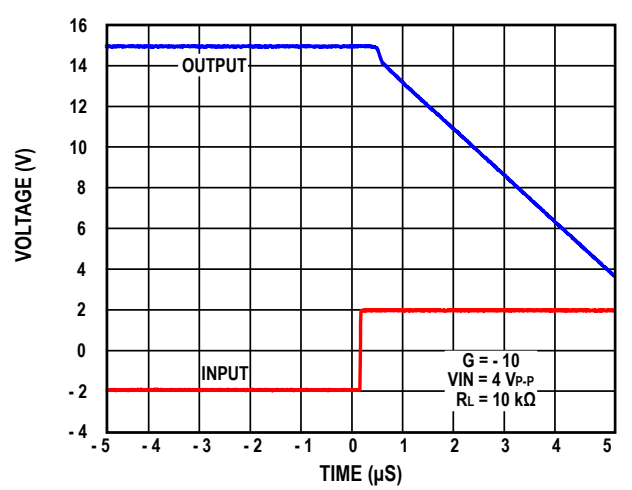


Figure 21. Negative Overload Recovery

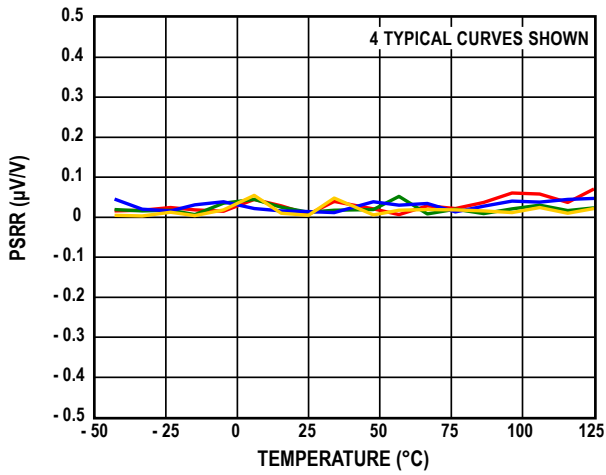


Figure 22. Power Supply Rejection Ratio (PSRR) vs. Temperature

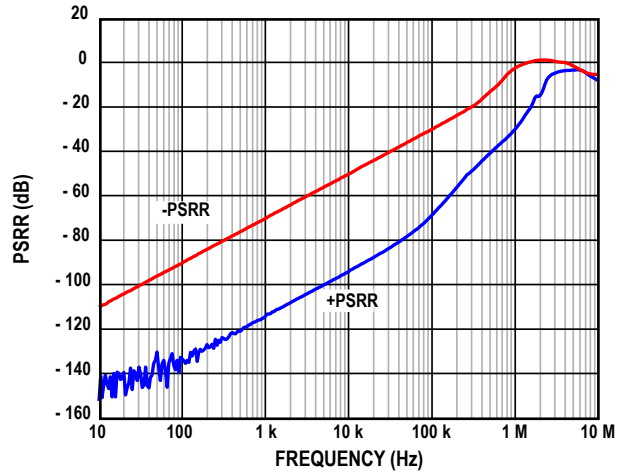


Figure 23. Power Supply Rejection Ratio (PSRR) vs. Frequency

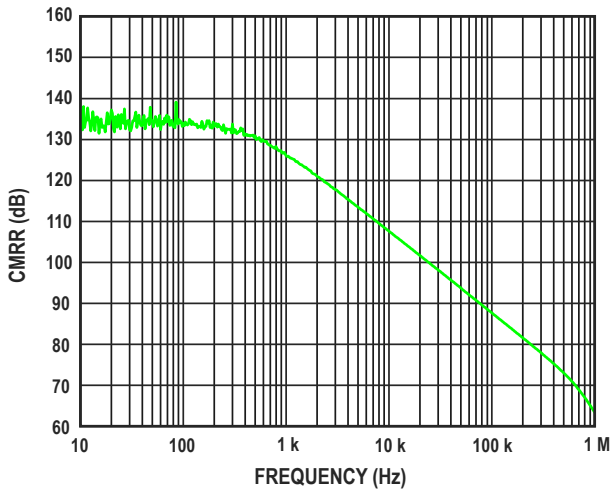


Figure 24. Common Mode Rejection Ratio (CMRR) vs. Frequency

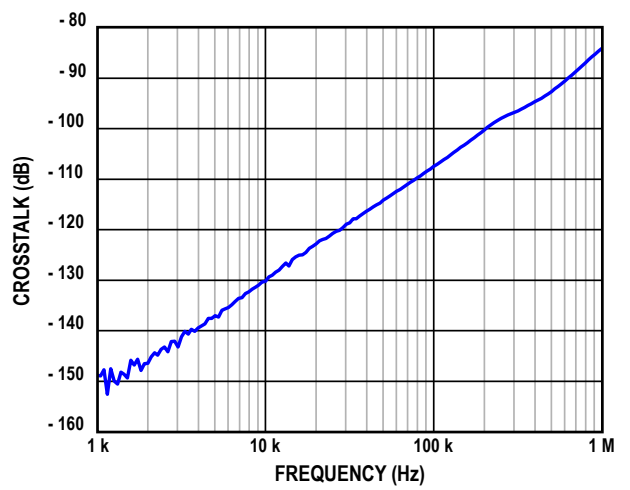


Figure 25. Channel Separation vs. Frequency

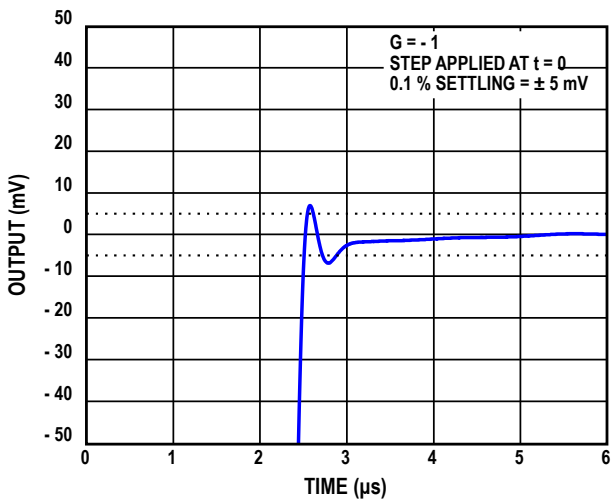


Figure 26. Positive Settling Time to 0.1%

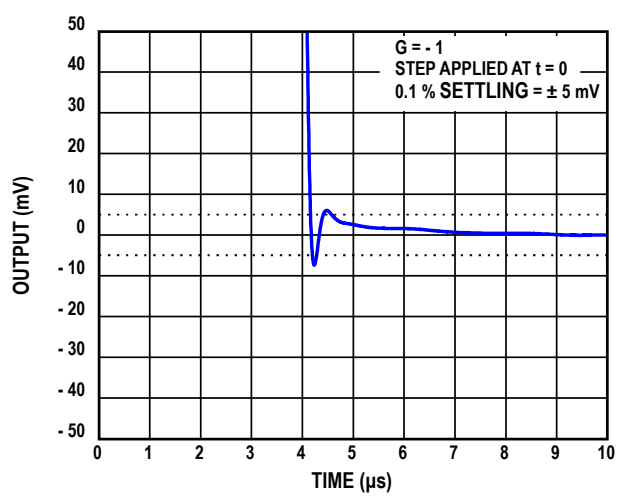


Figure 27. Negative Settling Time to 0.1%

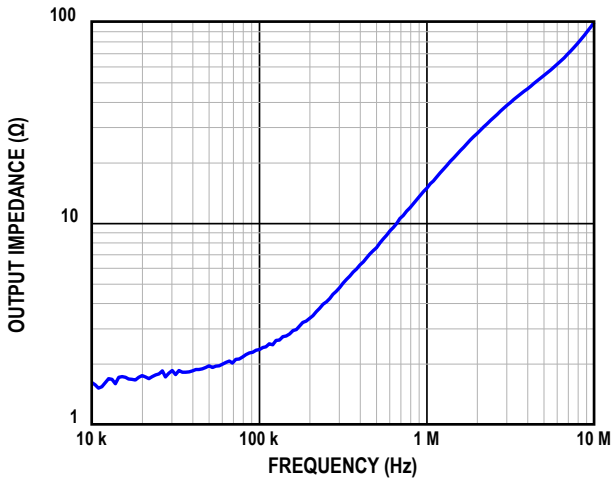


Figure 28. Output Impedance vs. Frequency

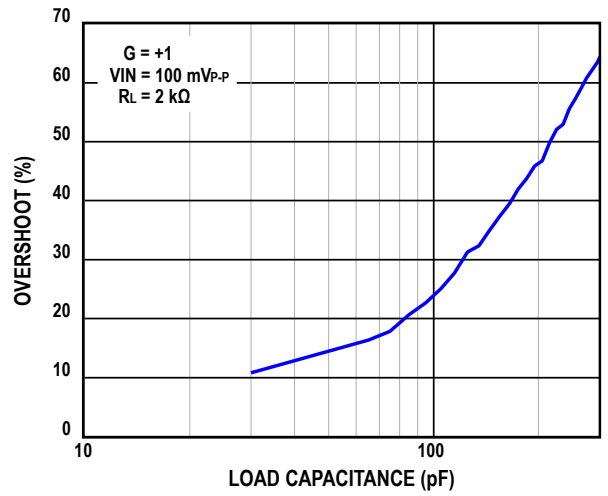


Figure 29. Small Signal Overshoot vs. Load Capacitance

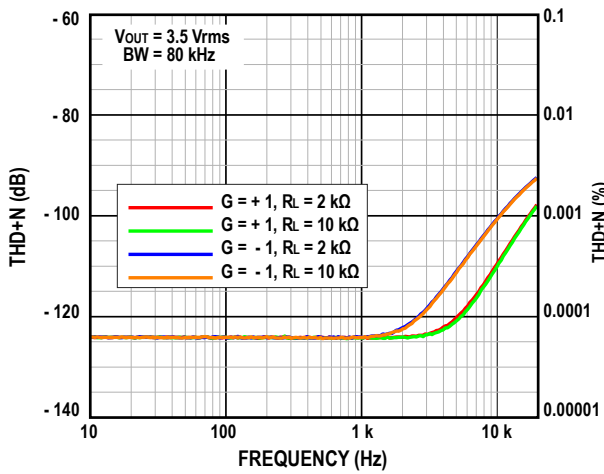


Figure 30. THD+N vs. Frequency

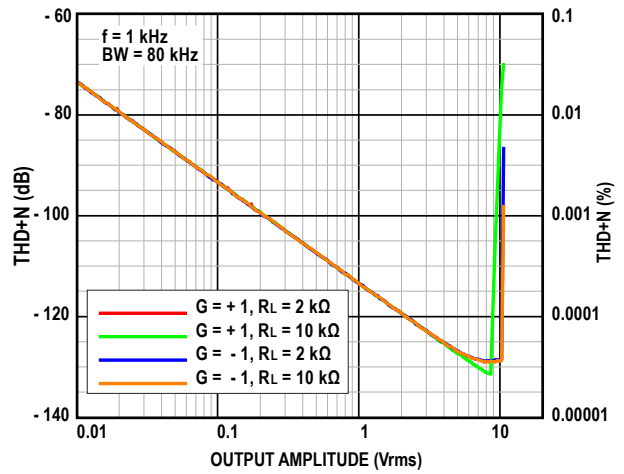


Figure 31. THD+N vs. Amplitude

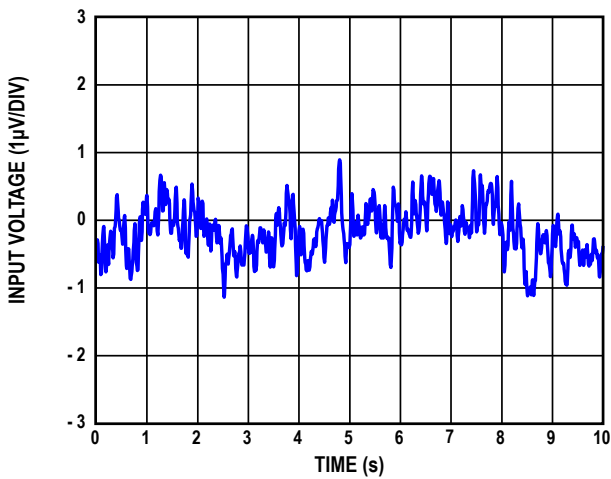


Figure 32. 0.1 Hz to 10 Hz Noise

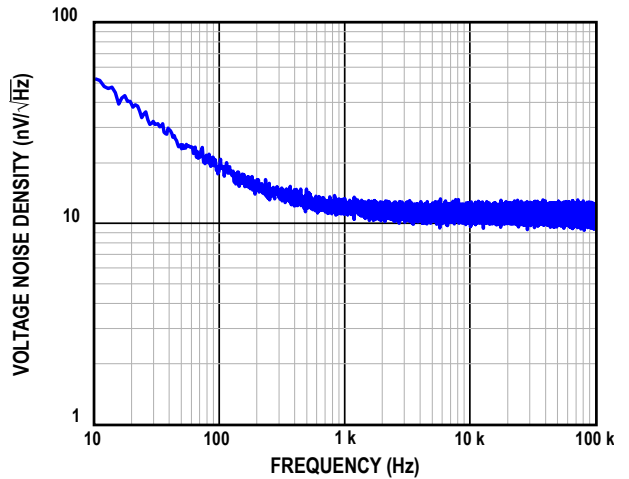


Figure 33. Voltage Noise Density vs. Frequency

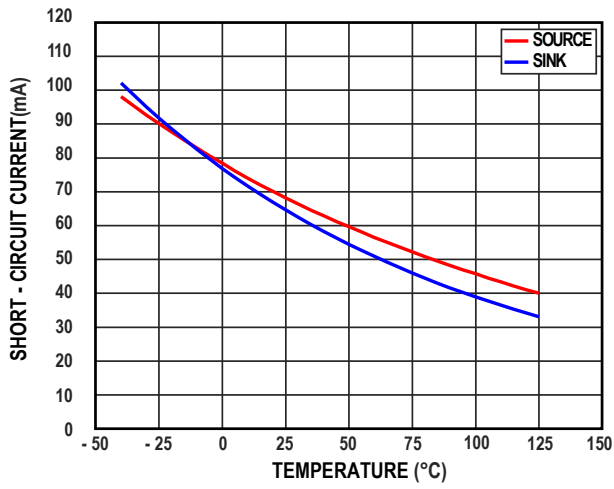


Figure 34. Output Short-Circuit Current vs. Temperature

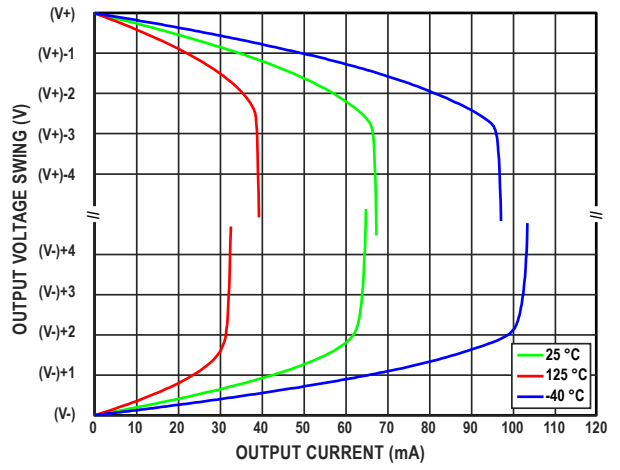


Figure 35. Output Voltage Swing vs. Output Current

## Theory of Operation

### Post-package Trimming

The ZJA3001 precision operational amplifier boasts a carefully designed MOS input stage, enabling it to maintain an exceptionally low input current of 25 pA maximum at 25 °C. Taking precision to the next level, the ZJA3001 employs ZJW's proprietary post-package trimming technology ZHIJINGTRIM®. This innovative approach involves fine-tuning adjustments (as shown in Figure 36), offering distinct advantages over traditional laser trimming techniques used at the wafer test stage. This post-package trimming method not only minimizes inherent process variations introduced during wafer manufacturing, but also significantly reduces additional defects potentially generated during the plastic molding process. Ultimately, the trimming results in the ZJA3001's exceptional performance: ultra-low offset voltage (35 μV maximum at 25 °C) and ultra-low offset voltage drift (0.5 μV/°C maximum across the specified temperature range in SOIC-8 package). Furthermore, ZJA3001 delivers consistent high accuracy cross wide supply voltage range from 4.5 V to 36 V. These remarkable characteristics make the ZJA3001 the ideal choice for demanding applications, such as high-impedance sensors interface, precision filtering and high-voltage high-precision data acquisition.

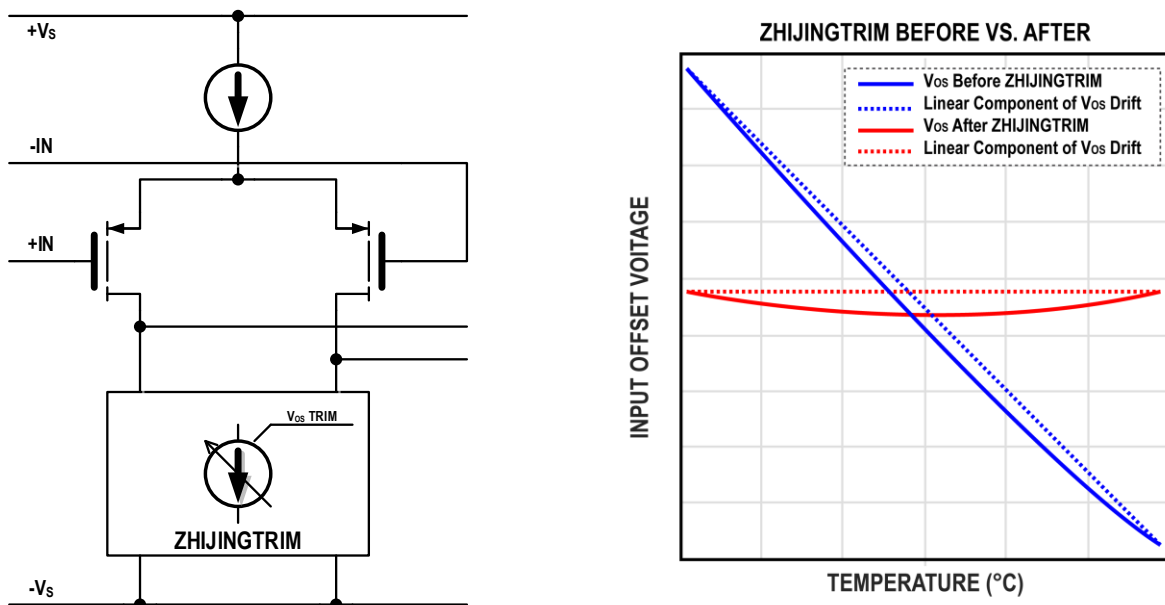


Figure 36. Diagram of Post-package Trimming Scheme (Left) and Effect (Right)



## Applications Information

### Source Impedance, Input Bias Current Affect both Output Noise and System Offset Voltage

As shown in Figure 37, the output noise density of classic bipolar input stage amplifiers #1, #2, and ZJA3001 is depicted at the 1 kHz frequency point under various source impedances. Bipolar amplifiers typically have large input bias current, leading to significant input current noise. When the source impedance exceeds 100 k $\Omega$ , the system noise rapidly increases. In contrast, the ZJA3001 has exceptionally low input bias current, resulting in minimal input noise current, thus its noise contribution to the system is negligible. When the source impedance surpasses 10 k $\Omega$ , the system noise is mainly contributed by the source impedance, which appears in the graph as a straight line overlapping the black line representing the noise contributed by source impedance. Similarly, high source impedance can cause considerable system offset voltage and its temperature drift due to the amplifier's input bias current, input offset current, and their temperature drifts. These effects are common in bipolar input amplifiers and zero-drift amplifiers. The ZJA3001, however, leverages its exceptional low input current to fully guarantee low system offset voltage and its temperature drift.

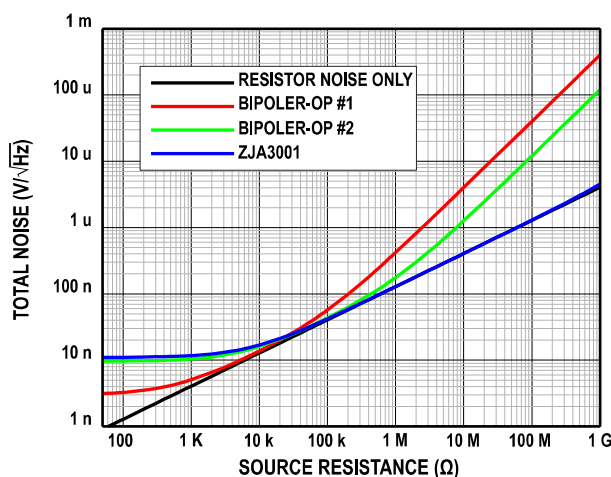


Figure 37. System Total Noise vs. Source Impedance

### Input Common Mode Voltage Range

While traditional bipolar amplifiers demand 1 V to 2 V of headroom from both supply rails for proper input common-mode voltage operation, often necessitating dual-supply configurations for applications with 0 V input common-mode signals. ZJA3001, in order to be compatible with it, also has the same input range. However, ZJA3001 has the ability to output to the rails, which can meet the needs of applications with a wider output range.

### Exceptional Linearity

Harnessing a proprietary linearity optimization design, the ZJA3001 achieves exceptional THD+N performance—reaching a remarkable minimum of -130 dB across the entire audio range and output amplitude, as shown in Figure 30 and Figure 31. This remarkable feat is made possible by its ultra-high open-loop gain, excellent frequency response, and extremely low noise characteristics.

### Output Phase Reversal

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal

when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ZJA3001 is immune to phase reversal problems even at input voltages beyond the supplies.

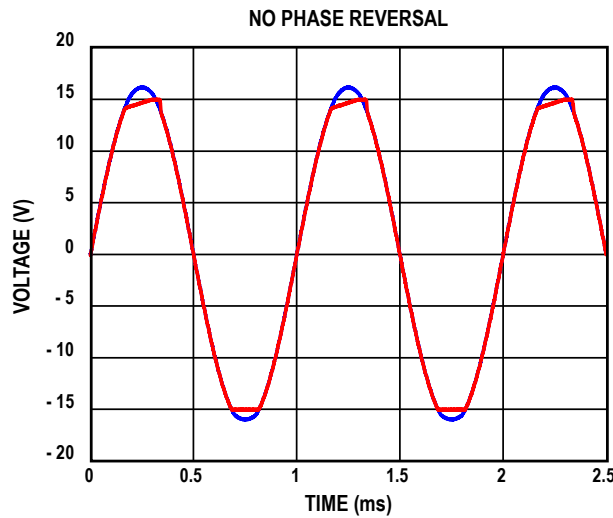


Figure 38. ZJA3001 Has No Output Phase Reversal

### Overload Recovery Time

Many zero-drift amplifiers, whether auto-zero or chopping, are plagued by a long overload recovery time, often in ms, due to the complicated settling behavior of the internal nulling loops after saturation of the outputs. Recovery time is important in many applications, particularly where the operational amplifier must amplify small signals in the presence of large transient voltages. The ZJA3001, as a continuous signal processing amplifier, stands out in this regard. Compared to zero-drift amplifiers, its overload recovery time is significantly shorter, falling within a remarkable 7  $\mu$ s, as demonstrably shown in the table below.

Model	Positive Overload Recovery ( $\mu$ s)	Negative Overload Recovery ( $\mu$ s)
ZJA3001	3.5	6.5
Competitor A	12.3	18

### Over Temperature Protection

Due to its high operating voltage (up to 36 V) and short-circuit current (up to 67 mA), the ZJA3001 can dissipate up to 2 W to 3 W of power during use. As thermal resistance for various package formats typically exceeds 100  $^{\circ}$ C/W, self-heating and the risk of permanent damage from high temperatures are concerns in real-world applications. To address this, the ZJA3001 incorporates an automatic over-temperature protection (OTP) function. When the chip temperature reaches 150  $^{\circ}$ C, OTP triggers, putting the chip into shutdown mode. Both input and output terminals enter a high-impedance state, significantly reducing power consumption and facilitating temperature drop. Once the chip cools down to 130  $^{\circ}$ C, OTP disengages, and the chip resumes normal operation.

### Input Bias Current Return Path

As shown in Figure 39, a simple AC coupling can be achieved by connecting a capacitor ( $C_{IN}$ ) in series between the non-inverting input (+) of the operational amplifier and the actual input ( $V_{IN}$ ) to isolate the DC voltage component of the input voltage. This coupling method is especially common in high-gain applications: when the gain is high, even a small DC voltage component at the amplifier input can affect the available output dynamic range of the op amp, and may even cause output saturation. However, for this AC coupling method located at the high-impedance input, if the input current of the positive input is not provided with a proper bias current return path, it will cause serious bias problems: in fact, the input bias current will slowly charge /discharge the capacitor  $C_{IN}$ , depending on the polarity of the input bias current, the capacitor will charge to the positive supply voltage or discharge to the negative supply voltage. This bias current caused offset voltage will be amplified by the op amp's closed-loop DC gain until the op amp's input voltage exceeds its input voltage range or the amplified output voltage exceeds its output voltage range, and this process may take a long time. For example, for an operational amplifier with an FET input stage, if its input current is 1 pA, through a 0.1  $\mu$ F capacitor, the offset voltage will be ramped at the speed of:

$$10 \text{ pA} / 0.1 \text{ } \mu\text{F} = 10 \text{ } \mu\text{V/s} = 0.6 \text{ mV/min} = 36 \text{ mV/h}$$

When the closed-loop DC gain is 100, the output voltage ramp rate is 3.6 V/h. Therefore, the actual circuit will not show obvious failure until after several hours. Using an AC coupled oscilloscope for a short-term test may not be able to find this problem.

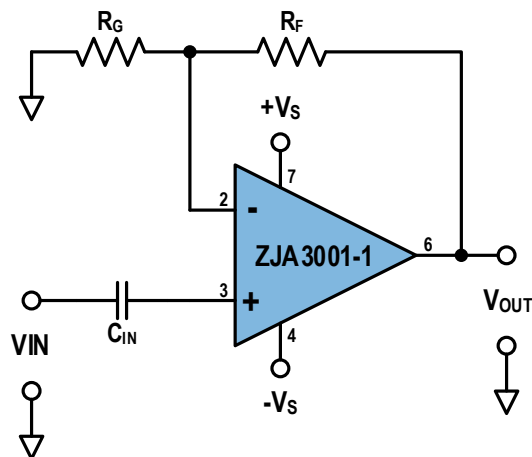


Figure 39. Incorrect AC-Coupled Op Amp Circuit

One simple solution is shown in Figure 40. A resistor ( $R_{IN}$ ) is connected between the input of the operational amplifier and ground, providing an input bias current return path. Unlike operational amplifiers with FET inputs, traditional bipolar operational amplifiers need to set  $R_{IN}$  to the parallel value of  $R_G$  and  $R_F$  to minimize the input offset voltage caused by input bias current, considering the mismatching between the two inputs of the op amp. Since this resistor will introduce additional noise to the overall circuit, the value of the input coupling capacitor and the resistor should be balanced between non-ideal factors such as input impedance, input high-pass cutoff frequency, and input offset voltage according to actual needs. Typical resistor value is generally between 100 k $\Omega$  and 1 M $\Omega$ .

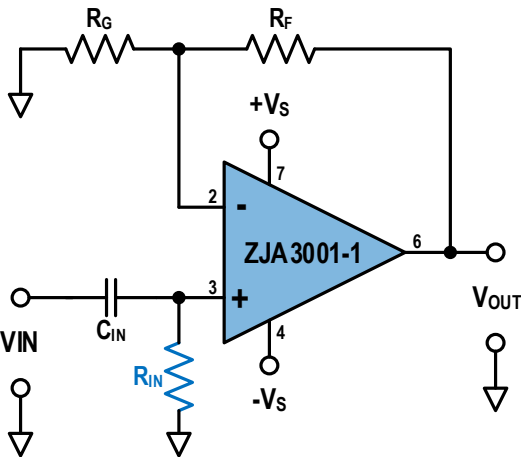


Figure 40. Creating an Input Bias Current Return Path

## Applications and Implementation

### Bandpass KRC Filter

The ZJA3001 series of amplifiers are particularly suitable for use in the design of precision filters, such as the typical KRC filter, as shown in Figure 41. With their excellent low offset and high CMRR performance, precision filters using ZJA3001 can guarantee stable performance over a wide input range while also having sufficient output dynamic range even at high gain. On the other hand, due to the ZJA3001-2/ZJA3001-4's ultra-high channel separation, even using the dual amplifiers in the same ZJA3001-2 can achieve excellent filter design without worrying about performance degradation caused by channel crosstalk.

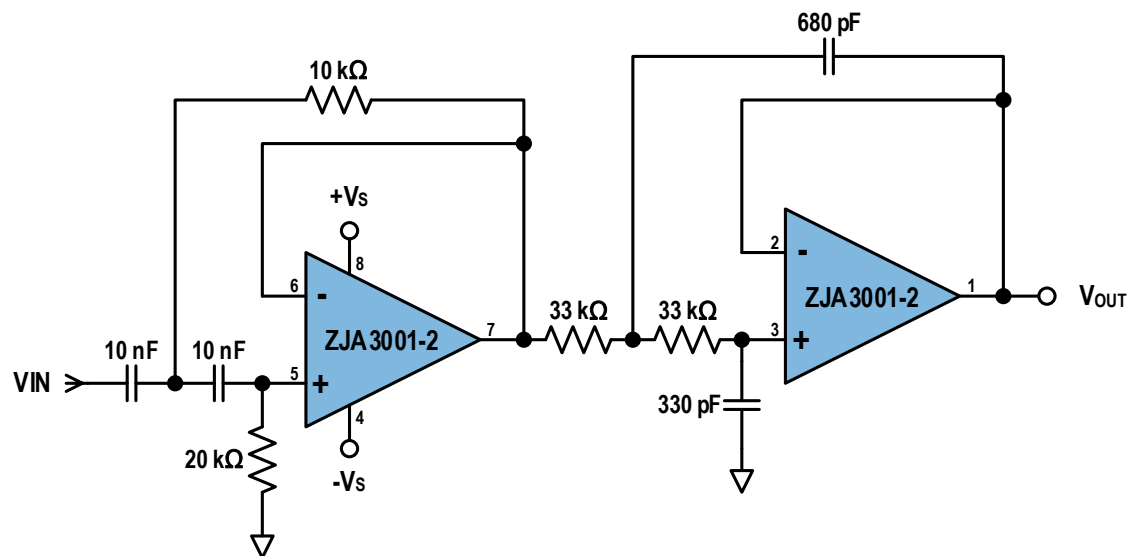


Figure 41. Using ZJA3001-2 to Build a 2-stage Band-pass KRC Filter

## Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 46, Figure 47, Figure 48 and Figure 49, keeping  $R_F$ ,  $R_G$  and  $C_F$  close to the inverting input minimizes parasitic capacitance.
  - Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85 °C for 30 minutes is sufficient for most circumstances.

Layout Example

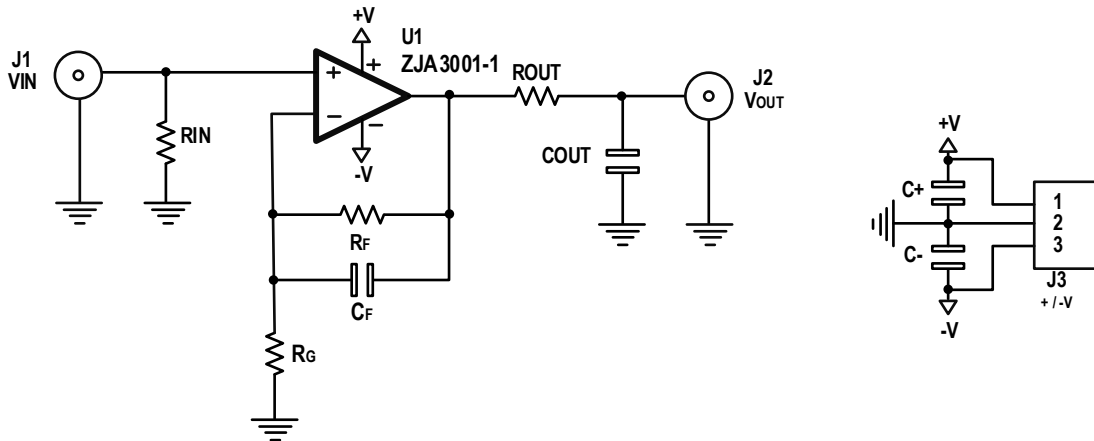


Figure 42. Op Amp Schematic for Non-inverting Configuration

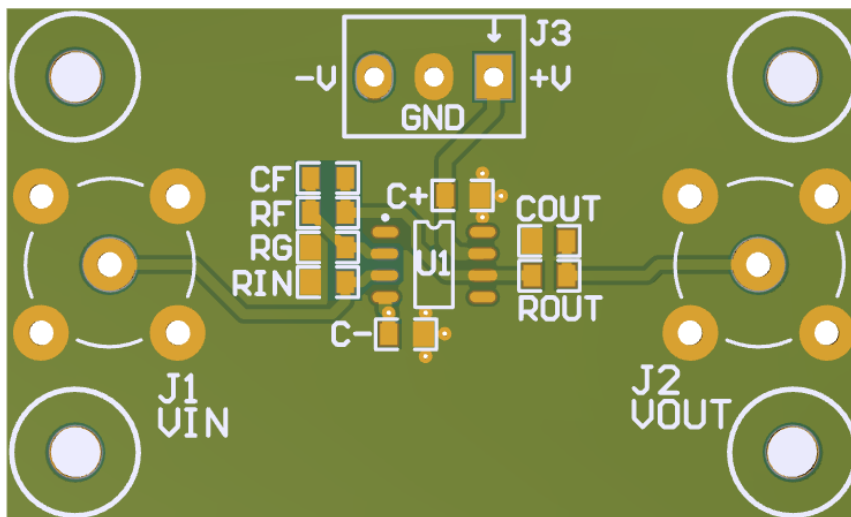


Figure 43. Layout of Op Amplifier in Non-Inverting Configuration (Silkscreen Layer)

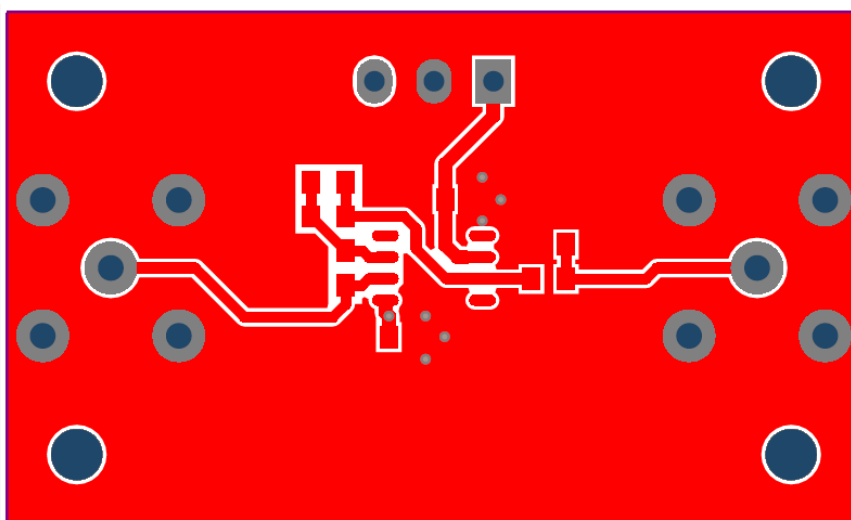


Figure 44. Layout of Op Amplifier in Non-inverting Configuration (Top Layer)

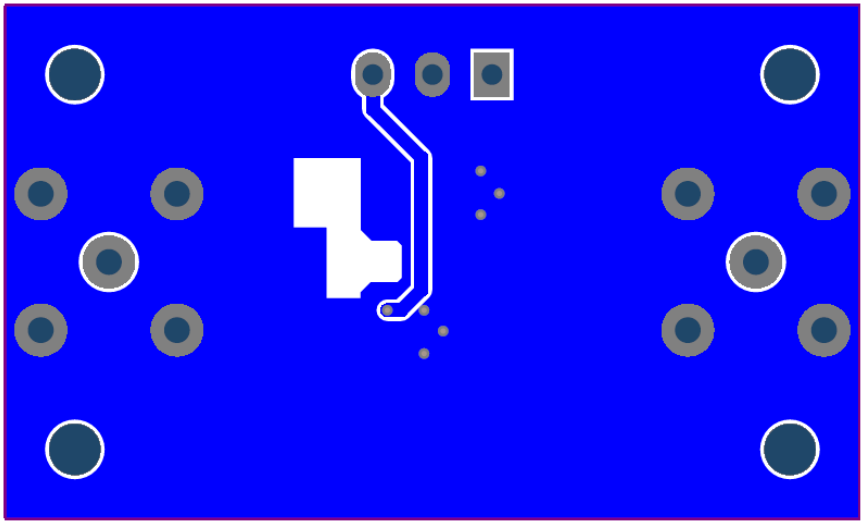


Figure 45. Layout of Op Amplifier in Non-inverting Configuration (Bottom Layer)



Outline Dimensions

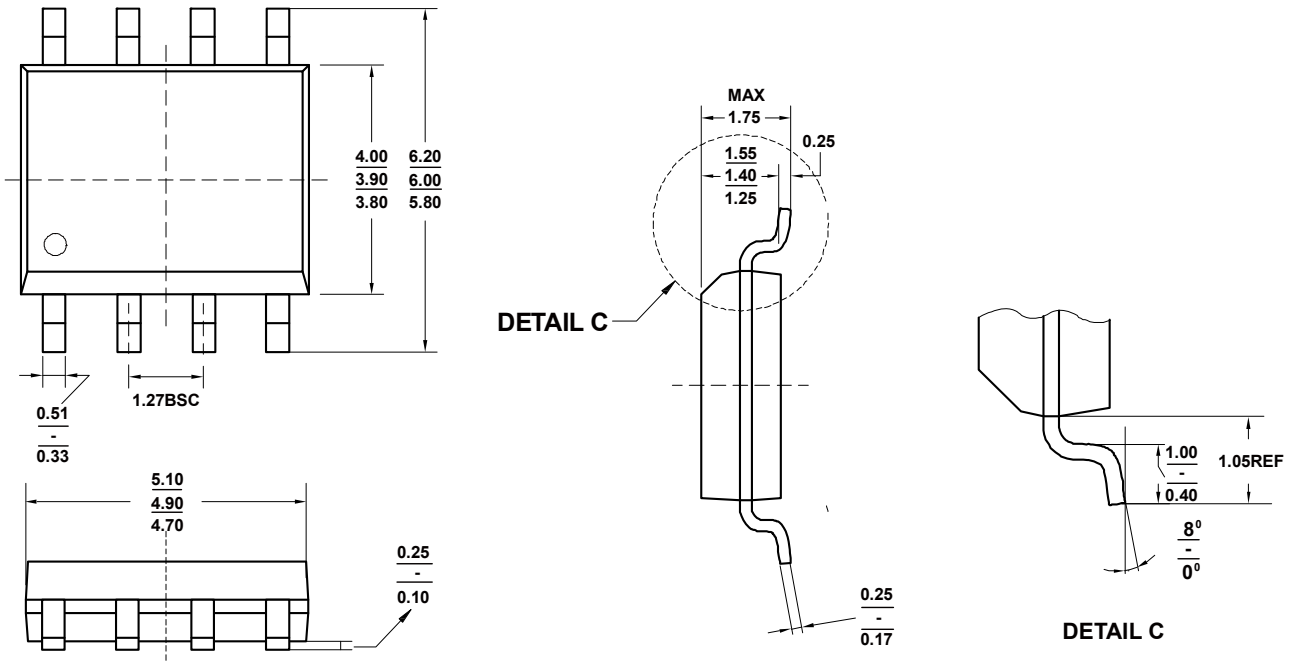


Figure 46. 8-Lead SOIC Package Dimensions shown in millimeters

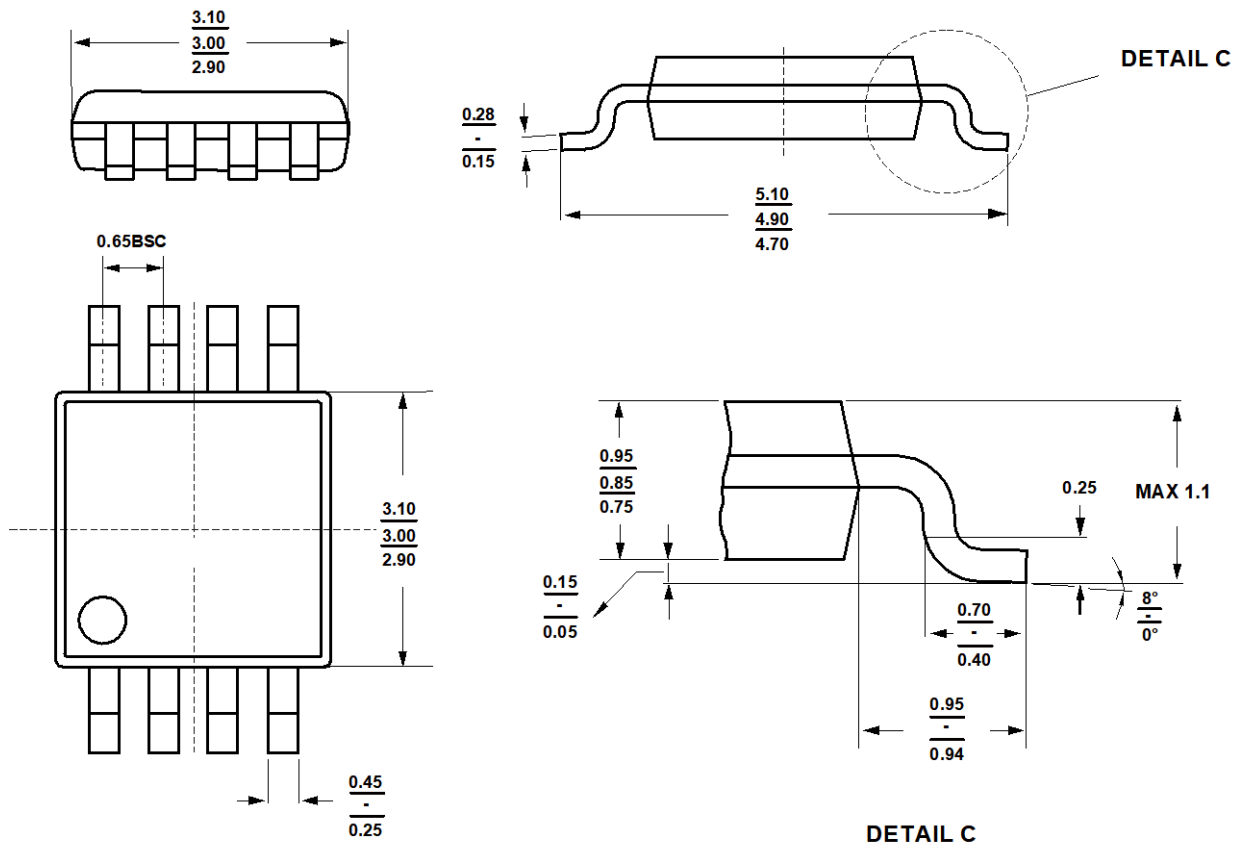


Figure 47. 8-Lead MSOP Package Dimensions shown in millimeters

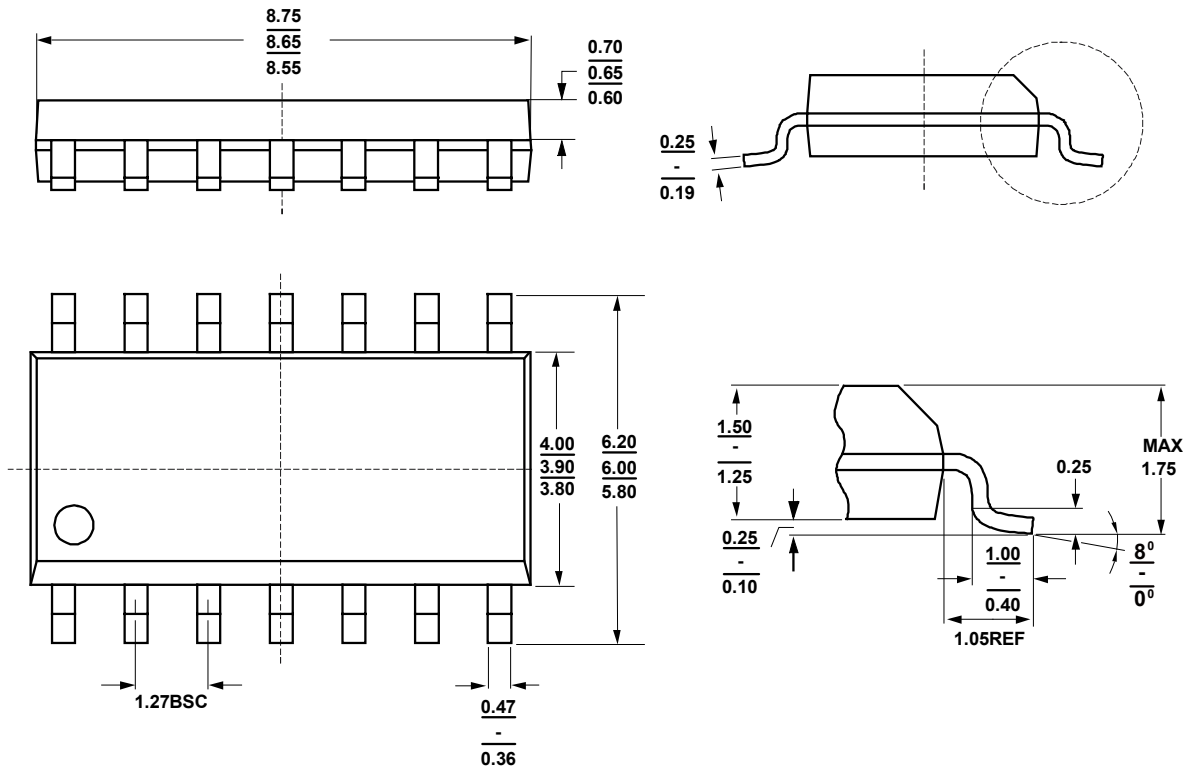


Figure 48. 14-Lead SOIC Package Dimensions shown in millimeters

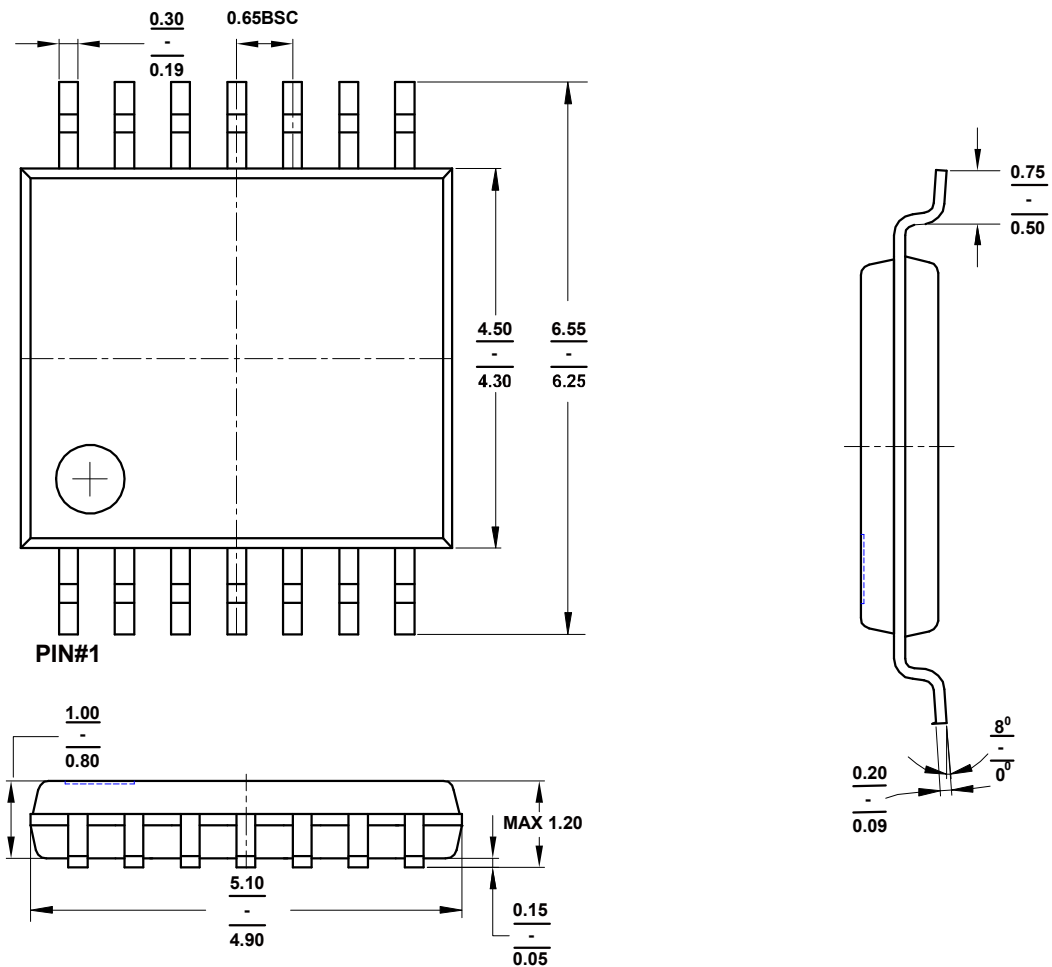


Figure 49. 14-Lead TSSOP Package Dimensions shown in millimeters

## Ordering Guide

Model	Orderable Device	Status <sup>1</sup>	Maximum Vos & TC <sub>Vos</sub>	Temperature Range (°C)	Package	External Package
ZJA3001-1	ZJA3001-1BSABT	ACTIVE	35 $\mu$ V & 0.5 $\mu$ V/°C	-40 to 125	SOIC-8	Tube
	ZJA3001-1BSABR	ACTIVE	35 $\mu$ V & 0.5 $\mu$ V/°C	-40 to 125	SOIC-8	13" reel
	ZJA3001-1ASABT	ACTIVE	35 $\mu$ V & 1.0 $\mu$ V/°C	-40 to 125	SOIC-8	Tube
	ZJA3001-1ASABR	ACTIVE	35 $\mu$ V & 1.0 $\mu$ V/°C	-40 to 125	SOIC-8	13" reel
	ZJA3001-1BUABT	ACTIVE	55 $\mu$ V & 0.8 $\mu$ V/°C	-40 to 125	MSOP-8	Tube
	ZJA3001-1BUABR	ACTIVE	55 $\mu$ V & 0.8 $\mu$ V/°C	-40 to 125	MSOP-8	13" reel
	ZJA3001-1AUABT	ACTIVE	55 $\mu$ V & 1.5 $\mu$ V/°C	-40 to 125	MSOP-8	Tube
	ZJA3001-1AUABR	ACTIVE	55 $\mu$ V & 1.5 $\mu$ V/°C	-40 to 125	MSOP-8	13" reel
ZJA3001-2	ZJA3001-2BSABT	ACTIVE	35 $\mu$ V & 0.5 $\mu$ V/°C	-40 to 125	SOIC-8	Tube
	ZJA3001-2BSABR	ACTIVE	35 $\mu$ V & 0.5 $\mu$ V/°C	-40 to 125	SOIC-8	13" reel
	ZJA3001-2ASABT	ACTIVE	35 $\mu$ V & 1.0 $\mu$ V/°C	-40 to 125	SOIC-8	Tube
	ZJA3001-2ASABR	ACTIVE	35 $\mu$ V & 1.0 $\mu$ V/°C	-40 to 125	SOIC-8	13" reel
	ZJA3001-2BUABT	ACTIVE	55 $\mu$ V & 0.8 $\mu$ V/°C	-40 to 125	MSOP-8	Tube
	ZJA3001-2BUABR	ACTIVE	55 $\mu$ V & 0.8 $\mu$ V/°C	-40 to 125	MSOP-8	13" reel
	ZJA3001-2AUABT	ACTIVE	55 $\mu$ V & 1.5 $\mu$ V/°C	-40 to 125	MSOP-8	Tube
	ZJA3001-2AUABR	ACTIVE	55 $\mu$ V & 1.5 $\mu$ V/°C	-40 to 125	MSOP-8	13" reel
ZJA3001-4	ZJA3001-4BSDBT	ACTIVE	35 $\mu$ V & 0.5 $\mu$ V/°C	-40 to 125	SOIC-14	Tube
	ZJA3001-4BSDBR	ACTIVE	35 $\mu$ V & 0.5 $\mu$ V/°C	-40 to 125	SOIC-14	13" reel
	ZJA3001-4ASDBT	ACTIVE	35 $\mu$ V & 1.0 $\mu$ V/°C	-40 to 125	SOIC-14	Tube
	ZJA3001-4ASDBR	ACTIVE	35 $\mu$ V & 1.0 $\mu$ V/°C	-40 to 125	SOIC-14	13" reel
	ZJA3001-4BUDBT	ACTIVE	55 $\mu$ V & 0.8 $\mu$ V/°C	-40 to 125	TSSOP-14	Tube
	ZJA3001-4BUDBR	ACTIVE	55 $\mu$ V & 0.8 $\mu$ V/°C	-40 to 125	TSSOP-14	13" reel
	ZJA3001-4AUDBT	ACTIVE	55 $\mu$ V & 1.5 $\mu$ V/°C	-40 to 125	TSSOP-14	Tube
	ZJA3001-4AUDBR	ACTIVE	55 $\mu$ V & 1.5 $\mu$ V/°C	-40 to 125	TSSOP-14	13" reel

<sup>1</sup> The marketing status values are defined as follows:

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**ACTIVE:** Product device recommended for new designs.

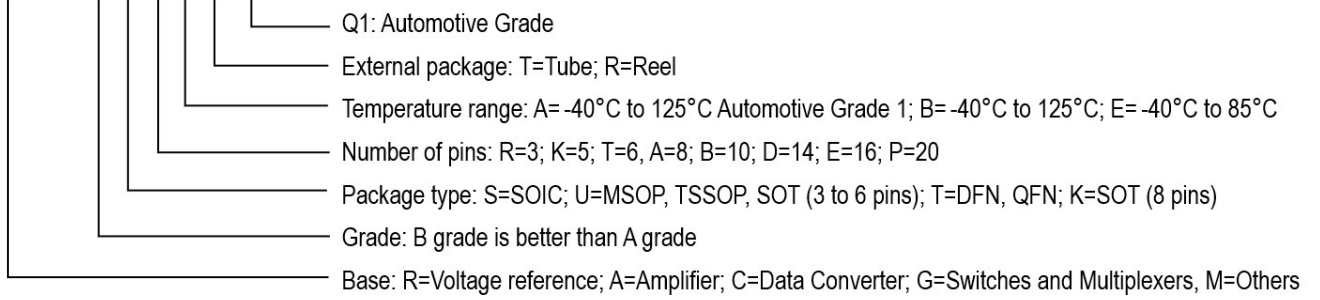
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.

**LIFEBUY:** ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**OBSOLETE:** ZJW has discontinued the production of the device.

Product Order Model

ZJXXXXX X X X X X Q1



## Related Parts

Part Number	Description	Comments
<b>ADC</b>		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2003/2013		Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2005/2015		Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB
ZJC2008/2018		Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB	
ZJC2100/1-16	16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2102/3-16	16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
ZJC2102/3-14	14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2104/5-16	16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
<b>DAC</b>		
ZJC2541-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2543-18/16/14		
ZJC2542-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
ZJC2544-18/16/14		
<b>Amplifier</b>		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 $\mu$ V max Vos, 0.5 $\mu$ V/ $^{\circ}$ C max TCvos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3001-1/2/4		
ZJA3018-2	OVP $\pm$ 75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 $\mu$ V max Vos, 0.5 $\mu$ V/ $^{\circ}$ C max TCvos, 25 pA max Ibias, 0.5 mA/ch, OVP $\pm$ 75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3008-2		
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/ $\mu$ S, 50 $\mu$ V max Vos, 1 $\mu$ V/ $^{\circ}$ C max TCvos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 $\mu$ V max Vos, 1 $\mu$ V/ $^{\circ}$ C max TCvos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 $\mu$ V max Vosi, $\pm$ 2.4 V to $\pm$ 18 V, -40 $^{\circ}$ C to 125 $^{\circ}$ C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G $\geq$ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 $\mu$ V max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to $\pm$ 65 V, CMRR 104 dB min (G = 1), Vos 100 $\mu$ V max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 $\mu$ A/channel, 2.7 V to 36 V
ZJA3678/9		
ZJA3669	High Common-Mode Voltage Difference Amplifier	$\pm$ 270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/ $\mu$ S, 50 nS to 16-bit, 50 $\mu$ V max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 $\mu$ V/ $^{\circ}$ C max TCvos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 $\mu$ V max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, $\pm$ 2.4 V to $\pm$ 18 V
<b>Voltage Reference</b>		
ZJR1004	40 V supply precision voltage reference	$V_{OUT} = 2.048/2.5/3.3/4.096/5/10$ V, 5 ppm/ $^{\circ}$ C max drift -40 $^{\circ}$ C to 125 $^{\circ}$ C
ZJR1001/2	5.5 V low power voltage reference (ZJR1001 with noise filter option)	$V_{OUT} = 2.048/2.5/3.3/4.096/5$ V, 5 ppm/ $^{\circ}$ C max drift -40 $^{\circ}$ C to 125 $^{\circ}$ C, $\pm$ 0.05% initial error, 130 $\mu$ A, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1003		
<b>Switches and Multiplexers</b>		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to $\pm$ 50 V power on & off, latch-up immune, Ron 270 $\Omega$ , 14.8 pC, tON 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 $\Omega$ , 14.8 pC charge injection, tON 166 nS
<b>Quad Matching Resistor</b>		
ZJM5400	$\pm$ 75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV