SiI9394 and SiI9679 HDMI/MHL 1, 2, 3 Bridge and Receiver with HDCP 2.2 Support

Data Sheet

SiI-DS-1146-B

February 2014

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General Description

The Silicon Image SiI9394 Mobile High-Definition Link (MHL®) 1, 2, 3 to High-Definition Multimedia Interface (HMDI®) bridge is an advanced integrated High-definition (HD) solution which can receive the latest MHL 1.x, MHL 2.x with High-bandwidth Digital Content Protection (HDCP) 1.4 encryption or MHL 3 with HDCP 2.2 encryption inputs, and support HDMI output with HDCP 1.4 or HDCP 2.2 encryption. The SiI9394 device can support up to 4K x 2K Ultra HD video format.

The SiI9679 HDMI/MHL 1, 2, 3 receiver is an advanced integrated High-definition (HD) solution which can receive the latest HDMI, MHL 1.x, MHL 2.x with HDCP1.4 encryption or HDMI, MHL 3 with HDCP2.2 encryption inputs, and support HDMI output with HDCP1.4 encryption. The SiI9679 device can support up to 4K x 2K Ultra HD video format.

The SiI9394 or the SiI9679 device implements MHL 3 eCBUS which supports SPI data tunneling and HSIC data tunneling.

General Features

- Support MHL 1.x, MHL 2.x, MHL 3 inputs, and HDMI output.
- Support SPI data tunneling. It implements Time Division Multiplexing (TDM) to hybrid Serial Peripheral Interface (SPI) data and legacy CBUS commands on the eCBUS-S or eCBUS-D.
- Support High-Speed Inter-Chip (HSIC) data tunneling. It implements TDM to hybrid the HSIC data and legacy CBUS commands on the eCBUS-S or eCBUS-D. The HSIC data is compliant with HISC specification.
- Support color space conversions among RGB, YCbCr 4:4:4, YCbCr 4:2:2 and xvYCC video formats without deep color.
- Support video format up to 4K x 2K @ 30 Hz with RGB/YCbCr 4:4:4/YCbCr 4:2:2, and up to 4k x 2k @ 60 Hz with YCbCr 4:2:0
- Support 3D frame sequential video format up to 1080p @ 60 Hz.
- Support high resolution VESA mode video format up to QSXGA @ 60 Hz.
- Support stand-alone mode with internal MCU controller and external MCU control mode.
- Integrated ISP module to support internal MCU firmware update through local I^2C interface.
- Low power 1.0 V core.

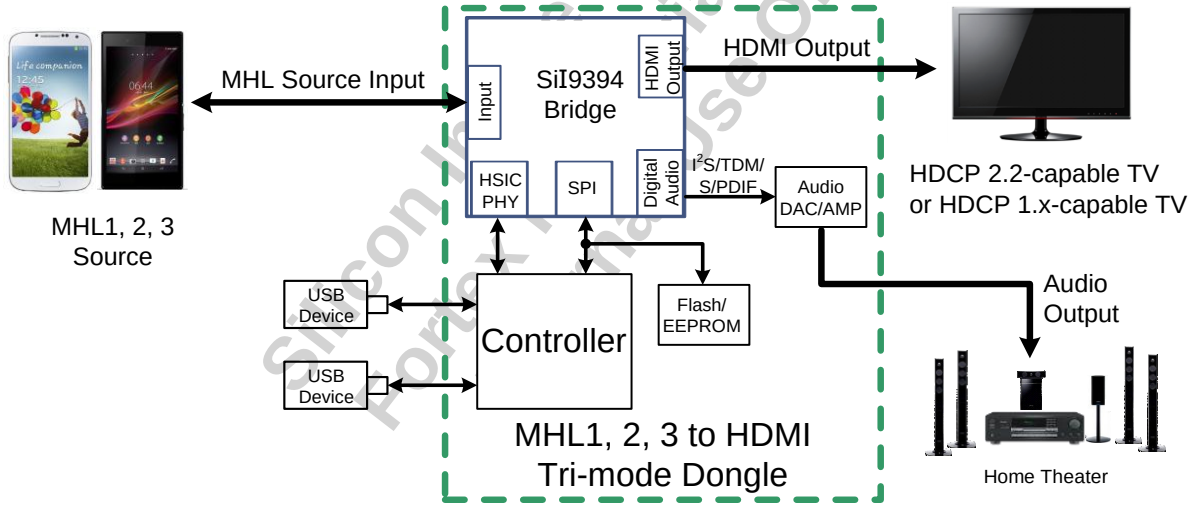


Figure 1. Typical Application for the SiI9394 Bridge

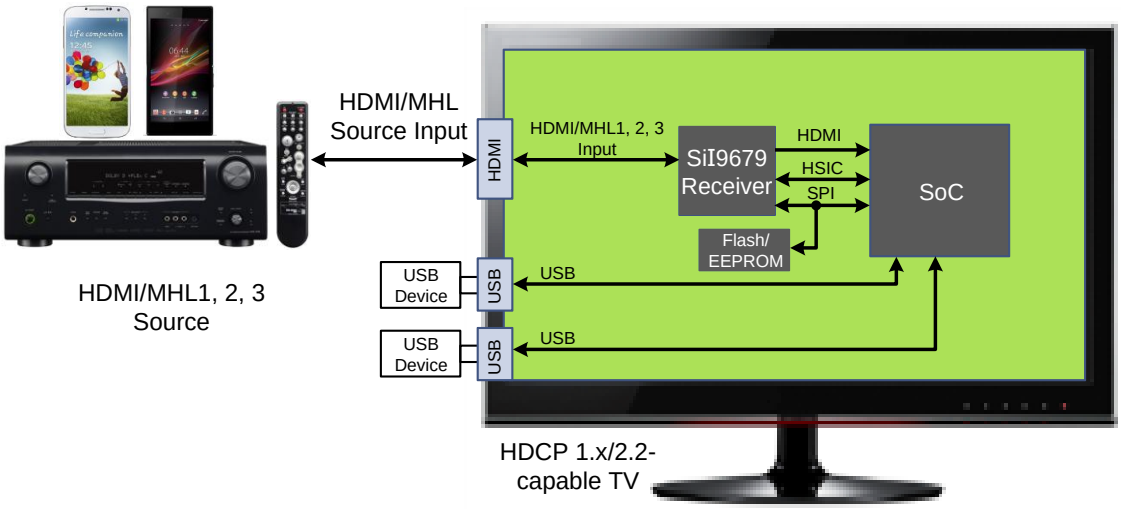


Figure 2. Typical Application for the SiI9679 Receiver

SiI9394 Bridge Only

- Support MHL 1.x, MHL 2.x, and MHL 3 inputs only.
- Support HDCP 2.2 and HDCP 1.x for both input and output ports.
- Support HDCP 2.2 repeater, HDCP 1.x repeater, and HDCP 2.2 to 1.x down-converter, and supports up to 127 downstream devices.
- Support Consumer Electronics Control (CEC) interface for HDMI output.
- Support audio extraction.
- One I^2S output lane supports two audio channels.
- TDM audio interface supports up to eight audio channels.
- S/PDIF output supports multichannel (5.1) Dolby Digital, DTS, MPEG2 Audio, and two-channel PCM (32 kHz – 192 kHz f_S sample rate).

SiI9679 Receiver Only

- Support HDMI and MHL 1.x, MHL 2.x, MHL 3 input.
- Support HDCP 2.2 and HDCP 1.x for input port.
- Support HDMI output without HDCP.
- Support optional HDCP 1.x output only for HDCP 2.2 input without repeater function.

Packaging

- 76-pin QFN (9 mm × 9 mm) package
- Standard part covers extended (–20 °C to +85 °C) temperature range.

Pin Diagram

Figure 3 shows the pin diagram of the SiI9394 device. Figure 4 on the next page shows the pin diagram of the SiI9679 device. The SiI9394/SiI9679 device is the 76-pin, 9 mm × 9 mm QFN package with an exposed pad (ePad). Refer to the Pin Descriptions on page 30 for a description of the pin functions.

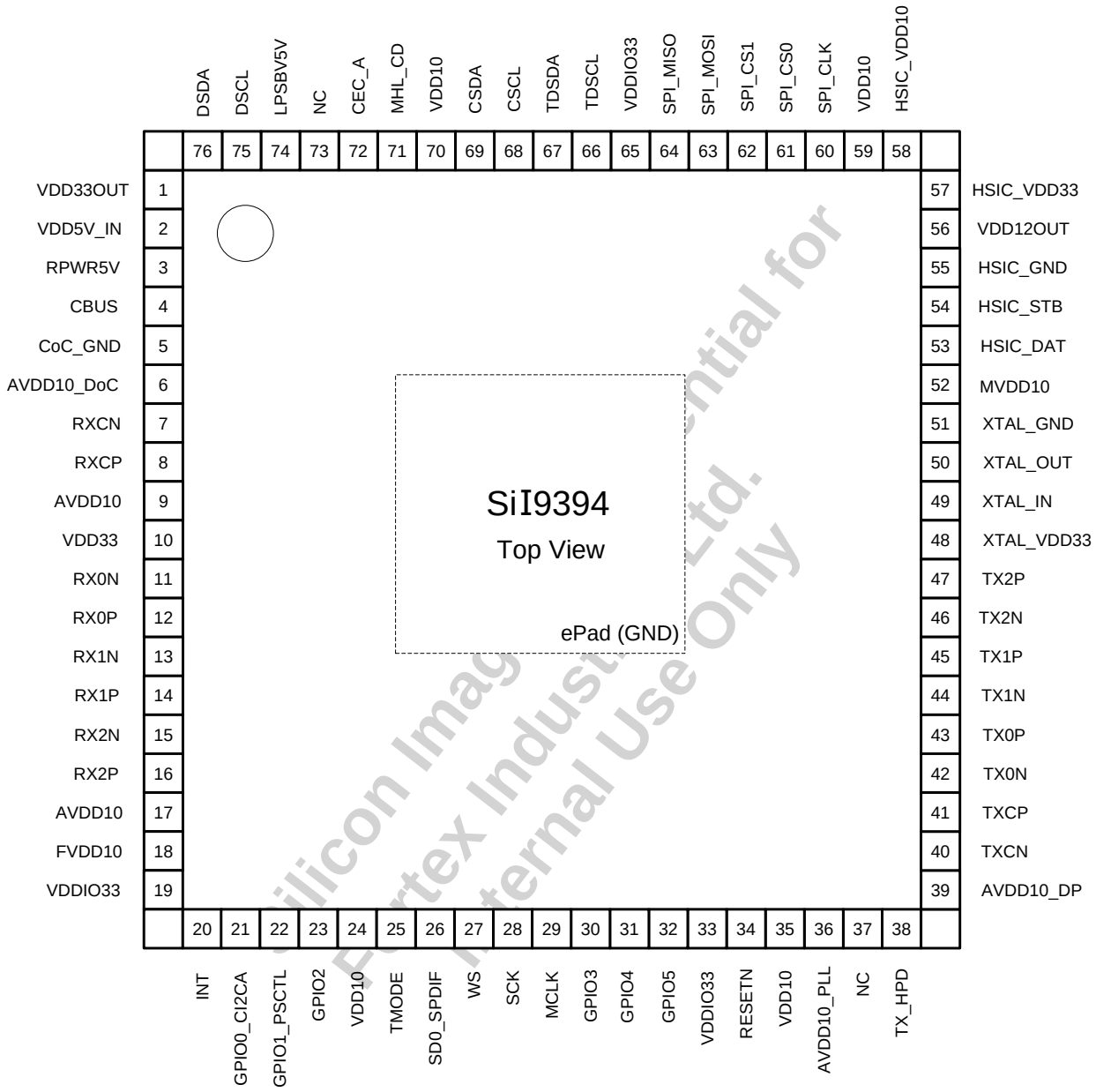


Figure 3. SiI9394 Pin Diagram

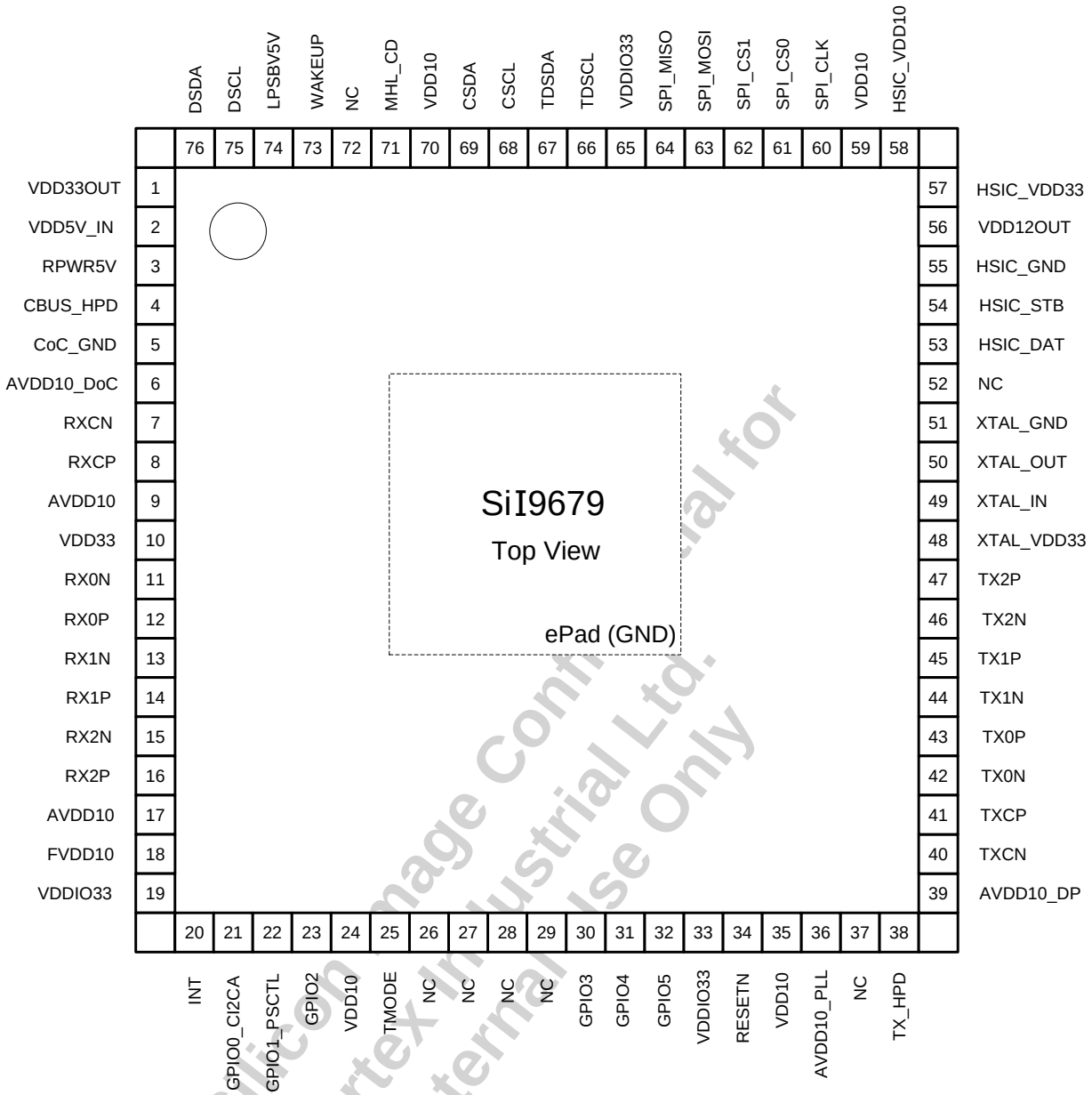


Figure 4. SiI9679 Pin Diagram

Functional Description

The SiI9394 bridge and the SiI9679 receiver can accept HDMI as well as MHL signals, sharing the same input interface. However, only one kind of input is available at a time. The MHL input signals include the MHL 1.x, MHL 2.x, MHL 3 (eCBUS-S) mode that has one differential TMDS lane and one single-end control bus, and MHL 3 (eCBUS-D) mode that has one differential TMDS lanes and one differential clock signal. When the SiI9394 or the SiI9679 device is in MHL 3 mode, the SiI9394 or the SiI9679 device can support data tunneling with HSIC and SPI interfaces. The SiI9394 or the SiI9679 device supports HDCP 1.x and HDCP 2.2.

The difference between the SiI9394 bridge and the SiI9679 receiver is that the SiI9394 bridge supports audio extraction and CEC function of the HDMI output interface, while the SiI9679 receiver does not. Figure 5 shows the functional block diagram of the chip.

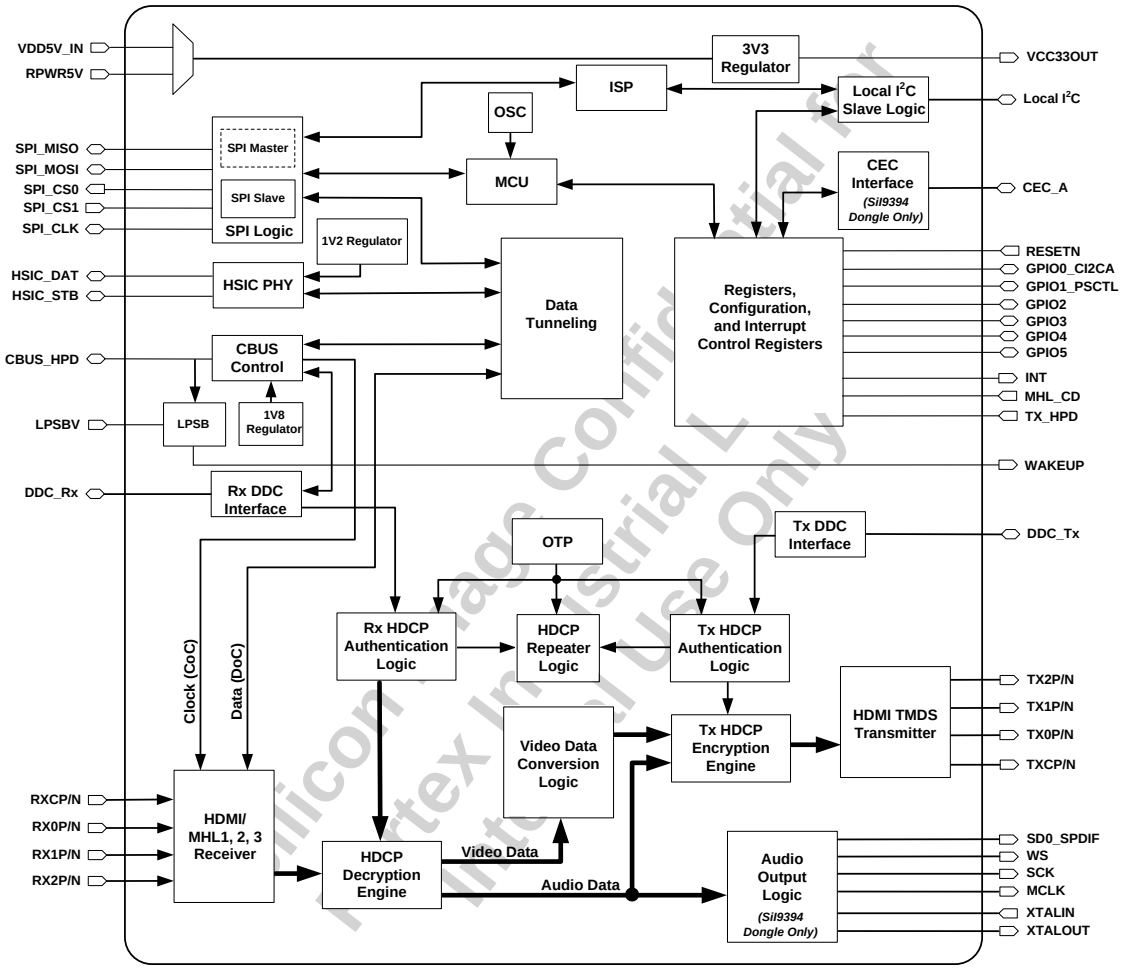


Figure 5. Functional Block Diagram

HDMI/MHL 1, 2, 3 Receiver Block

The HDMI/MHL 1, 2, 3 Receiver Block consists of HDMI, MHL 1.x, MHL 2.x, and MHL 3 interfaces. The working mode of the SiI9394 or the SiI9679 device depends on the type of source device that is connected to the input interface. The SiI9394 or the SiI9679 device selects the working mode of the receiver block automatically by detecting the status or actions of several pins, such as the RPWR5V, CBUS, or MHL_CD pin. In addition, the status of the discovery pulses on the CBUS is also to be considered. Refer to the corresponding MHL Specification section for details.

The HDMI/MHL 1, 2, 3 Receiver Block receives the TMDS signals and recovers the video, audio, and auxiliary data according to the working mode. For the MHL 3 (eCBUS-S) mode, the receiver block recovers the data with the link clock that is transmitted over the single-end eCBUS. For the MHL 3(eCBUS-D) mode, the receiver block recovers the data with the link clock that is transmitted over the differential eCBUS.

Table 1 shows the supported 2D formats. See the 3D Video Formats section on page 36 for details of the supported 3D formats.

Table 1. Supported 2D Video Formats

2D Video Resolution	Pixel Format	Bus Width			Maximum Frame Rate (Hz)
		HDMI	MHL 1.x/ MHL 2.x	MHL 3	
VGA	RGB	24	24	24	60
WVGA	RGB	24	24	24	60
SVGA	RGB	24	24	24	60
XGA	RGB	24	24	24	60
SXGA	RGB	24	No	24	60
UXGA	RGB	24	No	No	60
WUXGA	RGB	24	No	No	60
QXGA	RGB	24	No	No	60
WQXGA	RGB	24	No	No	60
480p/i	RGB YCbCr 4:4:4	24, 30, 36	24	24	60
	YCbCr 4:2:2	16, 20, 24	16	16	
576p/i	RGB YCbCr 4:4:4	24, 30, 36	24	24	50
	YCbCr 4:2:2	16, 20, 24	16	16	
720p	RGB YCbCr 4:4:4	24, 30, 36	24	24	50/60
	YCbCr 4:2:2	16, 20, 24	16	16	
1080i	RGB YCbCr 4:4:4	24, 30, 36	24	24	50/60
	YCbCr 4:2:2	16, 20, 24	16	16	
1080p	RGB YCbCr 4:4:4	24, 30, 36	24	24	24/30
	YCbCr 4:2:2	16, 20, 24	16	16	
1080p	RGB YCbCr 4:4:4	24, 30, 36	No	24	50/60
	YCbCr 4:2:2	16, 20, 24	16 (PackedPixel)	16	
4K x 2K	RGB YCbCr 4:4:4	24	No	No	24/25/30
	YCbCr 4:2:2	16, 20, 24	No	16 (PackedPixel)	
	YCbCr 4:2:0	12	No	No	50/60

Notes:

1. For the 4K x 2K YCbCr 4:2:0 format, no video data color space conversion is supported.
2. For deep color formats, no video data color space conversion is supported.

Video Data Conversion Logic Block

The SiI9394 bridge and the SiI9679 receiver device has a video data conversion logic block that is similar to that of other Silicon Image HDMI or MHL receiver products. Figure 6 shows the processing stages for the video data. Each of the processing blocks can be bypassed by setting the appropriate register bits.

The 4K x 2K YCbCr 4:2:0 @ 50/60 Hz video format and deep color video formats are not supported in the Video Data Conversion Logic Block. Therefore these formats will bypass this block.

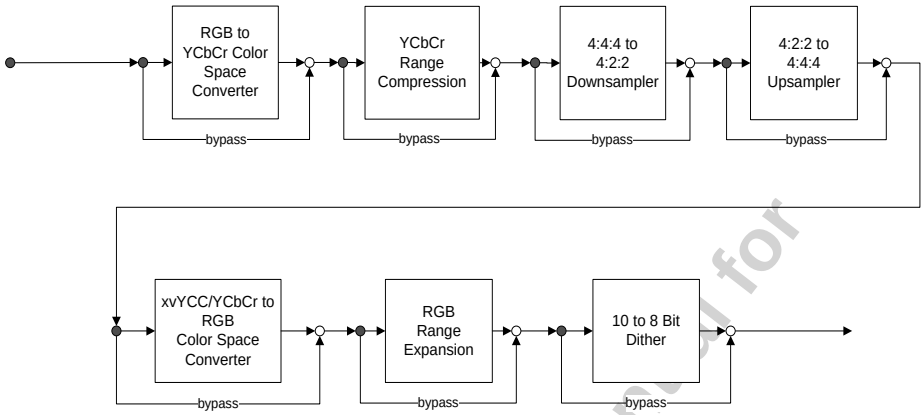


Figure 6. Default Video Processing Path

Color Space Converter

The Color Space Converter (CSC) converts RGB data to the Standard-Definition (ITU.601) or High-Definition (ITU.709) YCbCr formats, and vice-versa. To support the latest extended-gamut xvYCC displays, the SiI9394 or the SiI9679 device implements color space converter blocks to convert RGB data to the extended-gamut Standard-Definition (ITU.601) or High-Definition (ITU.709) xvYCC formats, and vice-versa. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

See the RGB to YCbCr Color Space Converter and YCbCr to RGB Color Space Converter sections on page 35 for more information.

xvYCC Support

The SiI9394 or the SiI9679 device adds support for the extended gamut xvYCC color space only in the HDMI mode. This extended format has roughly 1.8 times more colors than the RGB color space. The use of the xvYCC color space is possible because of the availability of LED and laser-based light sources for the next generation displays. This format also makes use of the full range of values (1 to 254) in an 8-bit space instead of 16 to 235 in the RGB format.

YCbCr Range Compression

When enabled by itself, the Range Compression Block compresses 0 – 255 full-range data into 16 – 235 limited-range data for each video channel, and compresses to 16 – 240 for the Cb and Cr channels. The color range scaling is linear.

4:4:4 to 4:2:2 Downsampler

Downsampling reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

4:2:2 to 4:4:4 Upsampler

Chrominance upsampling and downsampling increase or decrease the number of chrominance samples in each line of video. Upsampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

RGB Range Expansion

The SiI9394 or the SiI9679 device can scale the input color from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16 – 235 limited-range data into 0 – 255 for each video channel. When the range expansion and the xvYCbCr/YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16 – 240.

10 to 8 Bit Dither

The 10 to 8 Bit Dither block dithers internally processed 10-bit data to 8-bit data for output.

Receiver HDCP Authentication Logic Block

The Receiver HDCP Authentication Logic Block handles the task of establishing a secure link for receiving protected content from upstream device. This process involves exchanging security information with the source over the CBUS or DDC. The HDCP authentication logic has two parts: one is for HDCP 2.2 authentication, and the other is for HDCP 1.x authentication. The SiI9394 bridge and the SiI9679 receiver support different HDCP modes. Refer to the SiI9394 and SiI9679 Input and Output Matrix with HDCP section on page 36 for more details.

HDCP Decryption Engine Block

The SiI9394 or the SiI9679 device has two HDCP decryption engines: HDCP 2.2 decryption engine and HDCP 1.x decryption engine.

The HDCP Decryption Engine Block handles the task of decrypt data coming from the HDMI/MHL1, 2, 3 receiver blocks. The appropriate decryption key is applied to the HDCP decryption engine block to descramble the video, audio, and auxiliary packets.

The decryption mode can be configured by the device. Refer to the SiI9394 and SiI9679 Input and Output Matrix with HDCP section on page 36 for more details.

Transmitter HDCP Authentication Logic

The Transmitter HDCP Authentication Logic Block handles the task of establishing a secure link for transmitting protected content to downstream device. It also has two parts: one is for HDCP 2.2 authentication, and the other is for HDCP 1.x authentication. The authentication mode is determined by the configuration of the chip.

Unlike the HDCP 1.x authentication, the process for HDCP 2.2 involves authentication and key exchange, pairing for downstream device, random number generating, and locality check and session key exchange.

The SiI9394 bridge and the SiI9679 receiver support different HDCP modes. Refer to the SiI9394 and SiI9679 Input and Output Matrix with HDCP section on page 36 for more details.

HDCP Encryption Engine Block

The SiI9394 or the SiI9679 device has two HDCP encryption engines: HDCP 2.2 encryption engine and HDCP 1.x encryption engine.

The HDCP Encryption Engine Block contains the necessary logic to encrypt the incoming audio and video data and includes support for HDCP authentication. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes.

The decryption mode is configured by the device. Refer to the SiI9394 and SiI9679 Input and Output Matrix with HDCP section on page 36 for more details.

HDCP Repeater Block

The SiI9394 bridge supports HDCP 2.2 repeater, HDCP 1.x repeater, and HDCP 2.2 to 1.x down-converter.

The SiI9679 receiver supports HDCP 1.x output optional only for HDCP 2.2 input without repeater function.

The HDCP Repeater Block is only used when the chip is configured as a repeater, in which HDMI receiver and HDMI/MHL transmitter connections are cascaded. In this case, each transmitter has to ensure that all downstream receivers are HDCP-compliant. To ensure that all receivers in the downstream path are protected by HDCP, the downstream transmitters propagate a ready signal to the final upstream source transmitter.

One-Time Programmable (OTP)

The SiI9394 or the SiI9679 device comes preprogrammed with a set of production HDCP keys stored in an internal ROM. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. Silicon Image handles all purchasing, programming, and security for the HDCP keys. The pre-programmed HDCP keys provide the highest level of security because there is no way to read the keys once the devices are programmed. Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with Silicon Image before receiving samples of the device.

HDMI TMDS Transmitter Block

The HDMI TMDS Transmitter Block delivers an HDMI content stream, based on the content of the original stream from the source. Internal source termination eliminates the need to use external R-C components for signal shaping. The internal source termination can be disabled.

eCBUS Data Tunneling Block

The eCBUS Data Tunneling Block is used only for MHL 3 modes. In MHL 3 mode, the eCBUS data tunneling block implements the Time Division Multiplexing (TDM) to encode and decode the HSIC data, SPI data and legacy CBUS commands over eCBUS physical link, which can be used for eCBUS-S or eCBUS-D mode. Both modes support eCBUS data tunneling function with different bandwidth. The bandwidth of eCBUS-S is 75Mbps and eCBUS-D is 600Mbps.

The HSIC data is compliant with the HSIC Specification and the SPI data can include mouse, keyboard commands, and USB 1.1 data and so on. With this Data Tunneling Block, it realizes that the MHL 3 transmitter and receiver can exchange the SPI or the HSIC data through the MHL 3 interface. This block will transfer the SPI or HSIC data from or to the SPI Logic block or the HSIC PHY block accordingly.

CBUS Control Block

The CBUS Control Block handles the MHL Control Bus Interface. It is integrated with the CBUS controller of MHL 1.x, MHL 2.x, and MHL 3. The working mode of the CBUS control block is configured based on the input source type. The CBUS control block follows a specific communication and arbitration protocol to exchange EDID, Control, and HDCP information and so on.

In MHL 3 eCBUS-S mode, the Clock on CBUS (CoC) function will be supported. The link clock is carried on the eCBUS signal, which is fixed to 75 MHz. This link clock will be extracted in the CBUS Control Block, and sent to the HDMI/MHL1, 2, 3 Receiver Block for data recovery.

In MHL 3 eCBUS-D mode, the Data on Clock (DoC) function will be supported. The eCBUS commands are hybrid on the differential clock other than the legacy CBUS signal. Therefore, the CBUS Control Block will exchange the legacy eCBUS commands with the Data Tunneling Block, but not the CBUS signal. The CBUS signal is only used to handle the CBUS discovery process.

Low Power Standby Block

The Low Power Standby Block (LPSB) serves to minimize the power consumption while the device is in LPSB mode. This block is powered by LPSBV5V pin, which should be always powered. All other powers except LPSBV5V should be off when chip is in LPSB mode to minimize the leakage. LPSB block generates a wake up pulse through WAKEUP pin to the SoC to enable these power supplies when CBUS starts toggling or HDMI source is plugged in.

HSIC PHY

The HSIC PHY is used to communicate with the external System-On-Chip (SoC) for transmitting and receiving the HSIC data that will be sent on MHL 3 eCBUS. It offers 480 Mbps data traffic for the HSIC data that is compliant with HSIC specification.

SPI Logic Block

The SPI Logic Block has SPI Master and SPI Slave sharing the same interface. Only one interface is available at one time.

The SPI interface defaults to be an SPI Master and is sampled once after reset to load data from the external Flash when chip works in stand-alone mode. The SPI Master is also used when the In-System-Program (ISP) function block is enabled. Refer to the ISP Block section below for more details.

The SPI master and SPI slave use the same interface except the SPI Chip Select (SPI_CS) pins. The SPI_CS0 pin is only used for the SPI master, and the SPI_CS1 pin is only used for the SPI slave. Refer to the Data Tunneling Pins section on page 31 for details.

ISP Block

The SiI9394 or the SiI9679 device supports ISP for firmware upgrade. The ISP Block provides a connection between the Local I^2C Slave Logic and the SPI Master Logic. The firmware code is stored in the external Flash device that connected to the SPI interface. With this ISP block, the external SoC can program the latest code into the external Flash device directly through the local I^2C slave interface. The memory size of SPI Flash should not less than 100 kB.

Microcontroller Unit

The SiI9394 or the SiI9679 device has an embedded Microcontroller Unit (MCU) that provides a low-cost system implementation. It is used to control the main data flow by register configuration and interrupt handling, as well as handle the initialization at reset, HDCP 1.x/2.2 authentication and encryption and so on. This internal MCU will boot from the external Flash through the SPI master interface.

Internal Oscillator

The SiI9394 or the SiI9679 device has an Internal Oscillator (OSC) that provides the driving clock of the internal MCU for stand-alone mode. The frequency of this oscillator is 20 MHz, which is calibrated in the factory. In addition, the internal MCU can also use the external crystal as the clock source.

Local I^2C Slave Logic Block

The local I^2C slave bus provides a communication interface from the host to the SiI9394 or the SiI9679 device. The controller I^2C interface on the SiI9394 or the SiI9679 device (signals CSCL and CSDA) is a slave interface capable of running up to 400 kHz (see parametric limitation above 100 kHz in Table 25 on page 26). The host uses this interface to configure the SiI9394 or the SiI9679 device by reading from and writing to appropriate registers.

I^2C addresses of the device can be altered with the level of the CI2CA/GPIO4/GPIO5 signal, as described in the Device Address Configuration Using CI2CA/GPIO4/GPIO5 section on page 38.

Configuration, Status, and Interrupt Control Logic Block

The Configuration Block is used to configure and control the operation of the device, which can operate in either stand-alone mode (with internal 8051 enabled), or in External MCU mode.

The Power-On Reset (POR) circuit is also contained in this block. POR provides an on-chip reset function to eliminate the need of an external POR circuit.

The level on INT pin is latched when the POR transitions from the asserted state to the deasserted state. If the latched status is HIGH, the stand-alone mode is selected. Otherwise, External MCU mode is selected.

In the Stand-alone mode, the SiI9394 or the SiI9679 device requires an SPI flash/EEPROM for firmware code storage and loading the code to the internal MCU after the POR. All registers are configured by the internal MCU. This mode supports ISP function for firmware update.

In the External MCU mode, the SiI9394 or the SiI9679 device requires an external I^2C master such as MCU/SoC for register configuration.

Figure 7 and Figure 8 show the connection of the local I^2C port, SPI interface, and INT signal in stand-alone mode or in External MCU mode.

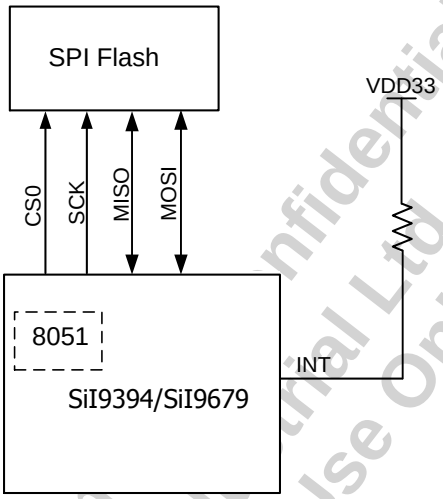


Figure 7. Stand-alone Mode

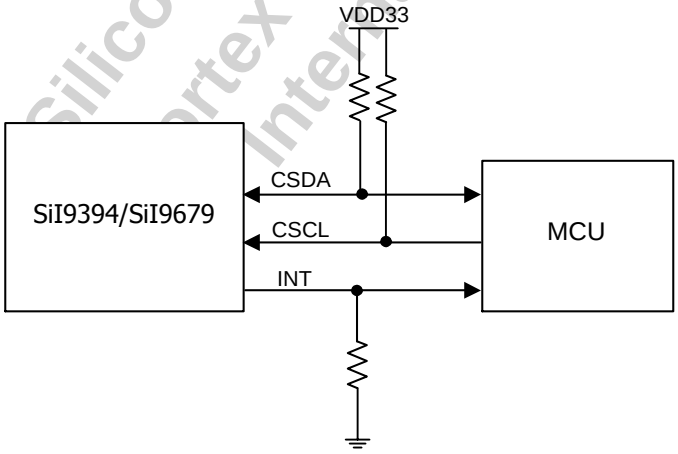


Figure 8. External MCU Mode

The INT signal interrupts the host processor when certain conditions arise inside the SiI9394 or the SiI9679 device. The INT output is programmable to be either active HIGH or active LOW pending on the operating mode.

For implementation, an API adapter driver is required by the hardware-independent interface between the SiI9394 or SiI9679 device and the application software. Refer to the SiI9394 Software API Reference document (SiI-AR-1000) for details.

Receiver DDC Interface

The Receiver DDC Interface provides a DDC master controller and a DDC slave controller.

In HDMI mode, the Receiver DDC Interface is used as a DDC slave for the HDMI source to read the EDID from the internal SRAM of the SiI9394 or the SiI9679 device and exchange the HDCP information.

In MHL mode, which includes MHL 1.x, MHL 2.x, and MHL 3 modes, the Receiver DDC Interface is also used to read the external EDID and exchange the HDCP information for the MHL source device. The data read from this DDC interface is encoded and decoded by the CBUS control block and sent over the legacy CBUS interface or the eCBUS to the MHL source device.

Transmitter DDC Interface

The Transmitter DDC Interface is a DDC Master for the HDMI downstream device connection. The DDC master port is used for direct connection to the HDMI cable. DDC read and write operations are executed by reading and writing registers in the device. This feature simplifies the system design and helps to lower its cost.

Audio Output Logic Block – SiI9394 Bridge Only

The SiI9394 device implements the Audio Output Logic Block to support the audio extraction function. It supports S/PDIF, two channel I^2S, and up to eight channels TDM audio interface as audio output. The pins for each format are shared. Thus only one audio interface is available at a time.

More information about audio support is available in the Audio Output Interface section on page 38.

The Audio Output Logic Block contains an Automatic Audio Configuration (AAC) logic that controls the audio output based on the current states of FIFO, Video, ECC, ACR, PLL, and InfoFrame. Audio output is enabled only when all necessary conditions are met. If any critical condition is missing, the audio output is disabled automatically.

CEC Interface Block – SiI9394 Bridge Only

The SiI9394 device supports the CEC interface for the HDMI output interface. The Consumer Electronics Control (CEC) Interface and CPI Register block provides CEC-compliant signals between CEC devices and a CEC master. This CEC controller has a high-level register interface accessible through the I^2C interface, which is used to send and receive CEC commands. The I^2C interface is compatible with the Silicon Image CEC Programming Interface (CPI). This controller makes CEC control easy and straightforward, removing the burden of requiring the host processor perform these low-level transactions on the CEC bus.

On-Chip Regulators

The SiI9394 or the SiI9679 device has two internal regulators: 3.3 V regulator and 1.2 V regulator. The on-chip regulators provide a low-cost system implementation.

The internal 3.3 V regulator is powered from the 5 V (RPWR5V or SBVCC5V) input and provides 3.3 V for internal use. The internal 1.2 V regulator provides 1.2 V for the internal HSIC PHY only. Each of the internal regulators has one output pin. The output pins are VDD33OUT and VDD12OUT. Neither pin can be used as an external power supply, however a separate 4.7 µF capacitor to ground is required for each pin.

Electrical Specifications

Absolute Maximum Conditions

Table 2. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
XTAL_VDD33	XTAL Power Supply	–0.3	—	4.0	V	1, 2, 3
HSIC_VDD33	HSIC Transceiver Power Supply	–0.3	—	4.0	V	1, 2
VDD33	Receiver Termination 3.3 V Analog Power Supply	–0.3	—	4.0	V	1, 2
VDDIO33	Digital I/O Power Supply	–0.3	—	4.0	V	1, 2
VDD10	Digital Core Power Supply	–0.3	—	1.25	V	1, 2
HSIC_VDD10	HSIC PHY Power Supply	–0.3	—	1.25	V	1, 2
AVDD10_DoC	Analog DoC (Data on Clock) Power Supply	–0.3	—	1.25	V	1, 2
AVDD10	Analog Receiver PHY Power Supply	–0.3	—	1.25	V	1, 2
AVDD10_PLL	Analog PLL Power	–0.3	—	1.25	V	1, 2
AVDD10_DP	Analog Data Path Power	–0.3	—	1.25	V	1, 2
FVDD10	Fractional PLL Power	–0.3	—	1.25	V	1, 2
MVDD10	Audio PLL Power	–0.3	—	1.25	V	1, 2
RPWR5V	5 V Input from Power Pin of HDMI Connector	–0.3	—	5.7	V	1, 2
VDD5V_IN	Local Power 5 V Input	–0.3	—	5.7	V	1, 2
LPSBV5V	Standby Power for Low Power Standby Mode	–0.3	—	5.7	V	1, 2
V_I	Input Voltage	–0.3	—	VDDIO33 + 0.3	V	1, 2
V_O	Output Voltage	–0.3	—	VDDIO33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V Tolerant Pins	–0.3	—	5.5	V	1, 2, 4
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. This is for 5V tolerant pins, such as TX_HPD, RX_HPD, DSCL, DSDA, INT, TDSCL, TDSDA, CSCL, CSDA, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, and GPIO5.

Normal Operating Conditions

Table 3. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
XTAL_VDD33	XTAL Power Supply	3.13	3.3	3.47	V	—
HSIC_VDD33	HSIC Transceiver Power Supply	3.13	3.3	3.47	V	—
VDD33	Receiver Termination 3.3 V Analog Power Supply	3.13	3.3	3.47	V	1
VDDIO33	Digital I/O Power Supply	3.13	3.3	3.47	V	—
VDD10	Digital Core Power Supply	0.95	1.0	1.05	V	—
HSIC_VDD10	HSIC PHY Power Supply	0.95	1.0	1.05	V	—
AVDD10_DoC	Analog DoC (Data on Clock) Power Supply	0.95	1.0	1.05	V	—
AVDD10	Analog Receiver PHY Power Supply	0.95	1.0	1.05	V	—
AVDD10_PLL	Analog PLL Power	0.95	1.0	1.05	V	—
AVDD10_DP	Analog Data Path Power	0.95	1.0	1.05	V	—
FVDD10	Fractional PLL Power	0.95	1.0	1.05	V	—
MVDD10	Audio PLL Power	0.95	1.0	1.05	V	—
RPWR5V	5 V Input from Power Pin of HDMI Connector	4.3	5.0	5.25	V	—
VDD5V_IN	Local Power 5 V Input	4.3	5.0	5.25	V	—
LPSBV5V	Standby Power for Low Power Standby Mode	4.75	5.0	5.25	V	—
V_{DDN}	Supply Voltage Noise	—	—	100	mV_{P-P}	2
T_A	Ambient Temperature (with power applied)	–30	+25	+85	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	28.0	°C/W	3
Θ_{jc}	Junction to Case Resistance (Theta JC)	—	—	14.4	°C/W	3

Notes:

1. The HDMI Specification requires termination voltage (VDD33) to be controlled to 3.3 V ± 5%.
2. The supply voltage noise is measured at test point VDDTP as shown in Figure 9. The ferrite bead provides filtering of power supply noise.
3. Airflow at 0 m/s, 4-layer PCB.

See the Power Supplies Decoupling section on page 41 for the recommended decoupling and power supply regulation.

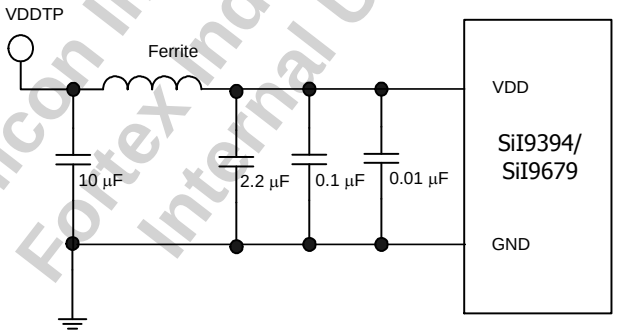


Figure 9. Test Point VDDTP for VDD Noise Tolerance Specification

DC Specification

Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Table 4. DC Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	Conditions[2]	Min	Typ	Max	Units	Notes
V_{IH}	HIGH Level Input Voltage	LVTTL	—	2.0	—	—	V	2
V_{IL}	LOW Level Input Voltage	LVTTL	—	—	—	0.8	V	2
V_{IH}	HIGH Level Input Voltage	HSIC	—	0.65 * V_{HSIC_VDD}	—	V_{HSIC_VDD} + 0.3	V	9
V_{IL}	LOW Level Input Voltage	HSIC	—	–0.3	—	0.35 * V_{HSIC_VDD}	V	9
V_{TH+DDC}	LOW to HIGH Threshold DDC BUS	Schmitt	—	3.5	—	—	V	5, 8
V_{TH-DDC}	HIGH to LOW Threshold DDC BUS	Schmitt	—	—	—	1.5	V	5, 8
V_{TH+CEC_A}	LOW to HIGH Threshold, CEC_A Pin	Schmitt	—	2.0	—	—	V	5
V_{TH-CEC_A}	HIGH to LOW Threshold, CEC_A Pin	Schmitt	—	—	—	0.8	V	5
$V_{TH+RESETN}$	LOW to HIGH Threshold RESETN pin	Schmitt	—	2.0	—	—	V	—
$V_{TH-RESETN}$	HIGH to LOW Threshold RESETN pin	Schmitt	—	—	—	0.8	V	—
V_{TH+I2C}	LOW to HIGH Threshold, I^2C Bus	Schmitt	—	2.0	—	—	V	—
V_{TH-I2C}	HIGH to LOW Threshold, I^2C Bus	Schmitt	—	—	—	0.8	V	—
V_{OH}	HIGH Level Output Voltage	LVTTL Open Drain	I_{OH} = 3 mA	2.4	—	—	V	—
V_{OL}	LOW Level Output Voltage	LVTTL Open Drain	I_{OL} = 3 mA	—	—	0.4	V	—
V_{OH}	HIGH Level Output Voltage	HSIC	—	0.75 * V_{HSIC_VDD}	—	—	V	9
V_{OL}	LOW Level Output Voltage	HSIC	—	—	—	0.25 * V_{HSIC_VDD}	V	9
O_D	I/O Pad Drive Strength	HSIC	—	40	—	60	Ω	—
Zi	I/O input Impedance	HSIC	—	240	—	—	KΩ	—
I_{IL}/I_{IH}	Input Leakage Current	—	—	–10	—	10	µA	—
TX_HPD I_{IL}/I_{IH}	Input Leakage Current	—	—	-30	—	30	µA	—
CEC_A, HSIC I_{IL}/I_{IH}	Input Leakage Current	—	—	-20	—	20	µA	—
I_{OD}	General Digital Output Drive	Output	V_{OH} = 2.4 V	7.5	—	—	mA	1, 6, 7
			V_{OL} = 0.4 V		—	—	mA	1, 6, 7

Notes:

1. These limits are guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading C_L = 10 pF.
3. Refer to the Pin Descriptions section on page 30 for pin type designations for all package pins.
4. Differential input voltage is a single-ended measurement, according to the DVI Specification.
5. Only these Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively and are guaranteed by design.

6. Minimum output drive specified at ambient = 70 °C and VDD33 = 3.0 V. Typical output drive specified at ambient =25 °C and VDD33 = 3.3 V. Maximum output drive specified at ambient = −20 °C and VDD33 = 3.6 V.
7. I_{OD} Output applies to all pins defined as LVTTL and LVTTL/Schmitt trigger.
8. I_{ODDDC} Output applies to all pins defined as Schmitt trigger.
9. V_{HSIC_VDD} is the internal 1.2 V HSIC signaling voltage, which supports 1.1 V - 1.3 V.

Table 5. TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	150	—	1200	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	V_{TERM} – 400	—	V_{TERM} – 37.5	mV
V_{ICM}	Common Mode Input Swing Voltage	—	150	—	1200	mV

Table 6. TMDS Input DC Specifications – MHL 1, 2 Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	V_{TERM} – 1200	—	V_{TERM} – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

Table 7. TMDS Input DC Specifications – MHL 3 Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	V_{TERM} – 1200	—	V_{TERM} – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

Table 8. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SWING}	Single-ended Output Swing Voltage	R_{LOAD} = 50 Ω	400	—	600	mV
V_H	Single-ended high-level Output Voltage	—	AVDD33 – 200	—	AVDD33 + 10	mV
V_L	Single-ended low-level Output Voltage	—	AVDD33 – 700	—	AVDD33 – 400	mV

CBUS I/O Specification

Table 9. Digital CBUS I/O Specifications

Symbol	Parameter	Signal	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	LOW to HIGH Threshold, CBUS pin	CBUS	—	1.0	—	—	V
V_{IL_CBUS}	HIGH to LOW Threshold, CBUS pin	CBUS	—	—	—	0.6	V
V_{OH_CBUS}	Output HIGH Voltage, CBUS pin	CBUS	85°C, I_{OH} = 300 µA	1.5	—	1.9	V
V_{OL_CBUS}	Output LOW Voltage, CBUS pin	CBUS	85°C, I_{OL} = 300 µA	—	—	0.2	V
I_{IL}	Input Leakage Current	CBUS	High Impedance	–1.0	—	1.0	µA
$Z_{CBUS\_SINK\_DISCOVER}$	Pull down resistance – Discovery	CBUS	—	800	1000	1200	Ω
$Z_{CBUS\_SINK\_ON}$	Pull down resistance – ON	CBUS	—	90	100	110	kΩ

DC Power Consumption

Table 10. Standby DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units	Notes
			5 V	3.3 V	1.0 V	5.25 V	3.47 V	1.05 V		
I_{DDLPSB}	Low power standby current	—	5.7	0	0	6.5	0	0	µA	1
I_{DDSB}	Standby current	—	7.4	10.1	160	8.1	8.7	365	mA	2

Notes:

1. Test under LPSB mode, only LPSBV5V is supplied and other power supplies are disabled.
2. All power nets are supplied and no input and output are connected.

Table 11. HDMI Input Mode DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units
			5 V	3.3 V	1.0 V	5.25 V	3.47 V	1.05 V	
I_{DDFP}	Full operation current	720x480p60	7.4	53.5	171	8.1	53.9	332	mA
		1920x1080p60	7.4	53.2	187	8.1	53.5	361	mA
		4Kx2Kp30	7.4	52.7	265	8.1	53.1	432	mA

Notes: Test results will differ pending on TMDS driving current settings of the source.

Table 12. MHL 1/2 Input Mode DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units
			5 V	3.3 V	1.0 V	5.25 V	3.47 V	1.05 V	
I_{DDFP}	Full operation current	720x480p	7.4	21.9	128	8.1	21.3	260	mA
		1280x720p60	7.4	21.9	141	8.1	21.3	270	mA
		1920x1080p60	7.4	21.1	169	8.1	21.2	283	mA

Notes: Test results will differ pending on TMDS driving current settings of the source.

Table 13. MHL 3 (eCBUS-S) Mode DC Power Consumption

Symbol	Parameter	Data Rate	Video Format	Typical			Maximum			Units
				5 V	3.3 V	1.0 V	5.25 V	3.47 V	1.05 V	
I_{DDFP}	Full operation current	6Gbps	720x480p60	21.4	16.1	252	22.1	16.4	423	mA
			1280x720p60	21.4	16.1	261	22.1	17.2	417	mA
			1920x1080p60	21.4	16.1	279	22.1	16.5	446	mA
			4Kx2Kp30	21.4	16.1	330	22.1	17.3	490	mA
		3Gbps	720x480p60	21.4	16.1	231	22.1	16.5	409	mA
			1280x720p60	21.4	16.1	240	22.1	16.5	415	mA
			1920x1080p60	21.4	16.1	245	22.1	17.2	432	mA
		1.5Gbps	720x480p60	21.4	16.9	186	22.1	17.3	399	mA
			1280x720p60	21.4	16.8	194	22.1	16.5	406	mA

Notes: Test results will differ pending on TMDS driving current settings of the source.

AC Specification

TMDS AC Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 14. TMDS Input Timings – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{INTRA-PAIR\_SKEW}$	Input Intrapair Skew	—	—	—	0.4	T_{BIT}
$T_{INTER-PAIR\_SKEW}$	Input Intrapair Skew	—	—	—	$0.2T_{PIXEL}$ + 1.78	ns
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz
T_{RXC}	Differential Input Clock Period	—	6.06	—	40	ns
T_{IJIT}	Differential Input Clock Jitter Tolerance	165 MHz	—	—	0.3	T_{BIT}

Table 15. TMDS Input Timings – MHL 1/MHL 2 Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{INTRA-PAIR\_SKEW}$	Input Intrapair Skew Tolerance	—	—	—	93	ps
F_{MHL}	MHL Link Clock Frequency	—	25	—	75	MHz
T_{MHL}	MHL Link Clock Period	—	13.3	—	40	ns

Table 16. TMDS Input Timings – MHL 3 (eCBUS-S) Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{INTRA-PAIR\_SKEW}$	Input Intrapair Skew Tolerance	—	—	—	93	ps
$F_{SE\_MHL\_CLK}$	Single-Ended MHL Link Clock Frequency	—	74.9625	75	75.0375	MHz
$T_{SE\_MHL\_CLK}$	Single-Ended MHL Link Clock Period	—	13.32	13.33	13.34	ns

Table 17. TMDS Input Timings – MHL 3 (eCBUS-D) Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{INTRA-PAIR\_SKEW}$	Input Intrapair Skew	—	—	—	25	ps
$F_{DF\_MHL\_CLK}$	Differential MHL Link Clock Frequency	—	149.925	150	150.075	MHz
$T_{DF\_MHL\_CLK}$	Differential MHL Link Clock Period	—	6663.33	6666.67	6670.00	ns

Note: Refer to the MHL Specification for more information on AC Specifications.

Table 18. TMDS Output Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TXDPS}	Intrapair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRT}	Data/Clock Rise Time	—	75	—	—	ps
T_{TXFT}	Data/Clock Fall Time	—	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DUTY}	Differential Output Clock Duty Cycle	—	40	—	60	T_{TXC}
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}

Audio Output Timings for the SiI9394 Bridge

Table 19. I^2S Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{TR}	SCK Clock Period (TX)	C_L = 10 pF	1.00	—	—	T_{TR}	Figure 13	1
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR}$ – 5	—	—	ns		1
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR}$ – 5	—	—	ns		1
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{TR}		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5	—	+5	ns		2
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. See Figure 13 on page 28. Meets timings in Philips I^2S Specification.
2. Applies also to SD-to-WS delay.

Table 20. TDM Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_TDM}	Sample Rate	2-8 Channel	32	—	192	kHz	—	2
T_{SCKCYC}	TDM SCK Cycle Time	C_L = 10 pF	—	1.0	—	UI	Figure 14	1
$T_{SCKDUTY}$	TDM SCK Duty Cycle	C_L = 10 pF	40	—	60	%UI		1
T_{TDMSU}	Setup Time, SCK to FS/SD	C_L = 10 pF	0.4UI – 3.5	—	—	ns		1
T_{TDMHD}	Hold Time, SCK to FS/SD	C_L = 10 pF	0.4UI – 3.5	—	—	ns		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–3.5	—	+3.5	ns		—
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. Proportional to unit time (UI), according to sample rate.
2. The video mode lower than 720p does not support multichannel 192 kHz sample rate.

Table 21. S/PDIF Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPCYC}	SPDIF Cycle Time	C_L = 10 pF	—	2.0	—	UI	Figure 15	1, 2
F_{SPDIF}	SPDIF Frequency	—	4	—	24	MHz		3
T_{SPDUTY}	SPDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI		2, 5
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20	—	250	ns	Figure 16	1, 2, 4
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4	—	50	MHz		1, 2, 4
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$		2, 4
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. SPDIF is not a true clock, but is generated from the internal 128 f_s clock, for f_s from 128 to 512 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its use as an S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1 UI.

Table 22. Audio Crystal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{XTAL}	External Crystal Frequency	—	26	27	28.5	MHz	Figure 10

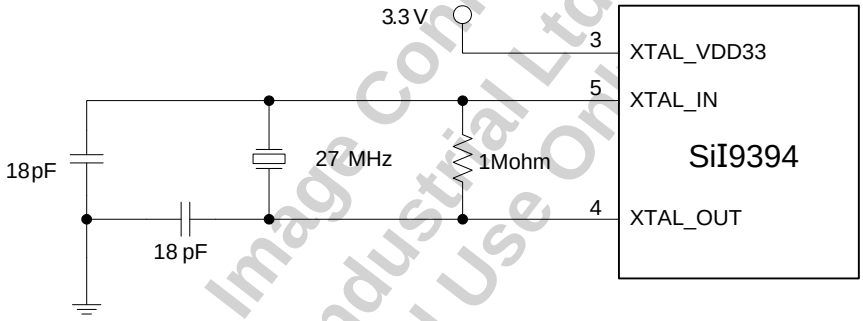


Figure 10. Audio Crystal Application

SPI Interface Timing

Table 23. SPI Control Signal Timings

Symbol	Parameter	Min	Typ	Max	Units	Figure
F_{SPI_CLK}	SPI_CLK Frequency	1.0	30	66	MHz	—
tCSs	SPI_CS_N Setup Time to SPI_CLK	1.05	—	—	ns	Figure 17, Figure 18
tCSh	SPI_CS_N Hold Time to SPI_CLK	1.25	—	—	ns	
tTXs	SPI_MOSI Setup Time to SPI_CLK	0.45	—	—	ns	
tTXh	SPI_MOSI Hold Time to SPI_CLK	2.0	—	—	ns	
tRXp	SPI_MISO Output Time from SPI_CLK Launch Edge	1.0	—	4.54	ns	Figure 18

Note: Under normal operating conditions otherwise specified.

HSIC Interface Timing

Table 24. HSIC Interface Control Signal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{STROBE}	Strobe Frequency	—	239.988	240	240.012	MHz	Figure 19
T_{SLEW}	Slew Rate (rise and fall)	—	0.7	1.0	1.2	V/ns	
T_S	Receiver data setup time	—	365	—	—	ps	
T_T	Transmitter uncertainty	—	—	—	365	ps	
T_H	Receiver data hold time	—	300	—	—	ps	

Miscellaneous Timings

Under normal operating conditions unless otherwise specified.

Table 25. Miscellaneous Timings

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	Delay from falling edge of I^2C clock that I^2C data is valid	C_L = 400 pF	—	—	700	ns	—	—
F_{DDC}	Speed on TMDS DDC port	C_L = 400 pF	—	—	100	kHz	—	2
F_{I2C}	Speed on local I^2C port	C_L = 400 pF	—	—	400	kHz	—	3
T_{RESET}	RESETN Signal LOW Time for valid reset	—	2	—	—	ms	Figure 11	—
T_{RESET_VDD}	Time required for RESETN high before VDD	50% RESETN to 90% VDD	1	—	—	µs	Figure 12	—

Notes:
1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. DDC port is limited to 100 kHz by the HDMI Specification, and meets I^2C Standard mode timings.
3. Local I^2C can operate up to fast mode 400 kHz speed.

ESD Specifications

Table 26. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
Latch up	ESD Latch up	± 200	—	—	mA	1, 2
HBM	Human Body Model	2000	—	—	V	3
MM	Machine Model	200	—	—	V	4
CDM	Charged Device Model	500	—	—	V	5

Notes:
1. Test is performed at 70 °C.
2. Measured according to JESD78B standard.
3. Measured according to JESD22-A114 standard.
4. Measured according to JESD22-A115 standard.
5. Measured according to JESD22-C101 standard.

Timing Diagrams

RESETN Timing Diagrams

Power sequencing is not required for the SiI9394 or the SiI9679 device. However, to ensure a proper reset the rules mentioned under the diagrams in Figure 11 and Figure 12 must be followed.

VCC must be stable between its limits for Normal Operating Conditions for T_{RESET_VDD} before RESETN goes HIGH, as shown in Figure 11. Before accessing registers, RESETN must be pulled low for T_{RESET}. This can be done by holding RESETN low until T_{RESET_VDD} after stable power, as described above, or by pulling RESETN LOW from a HIGH state for at least T_{RESET}, as shown in Figure 12.

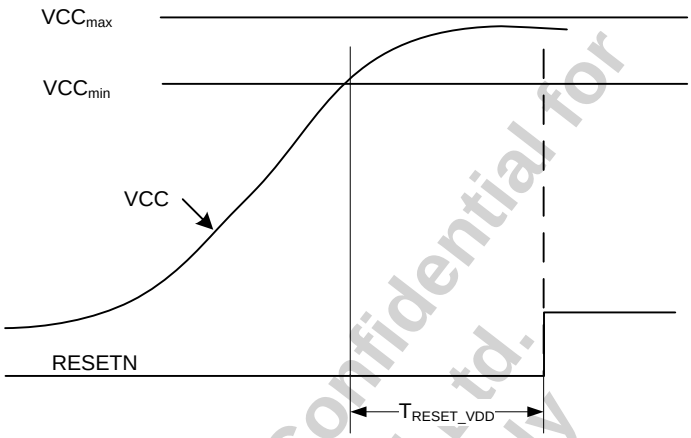


Figure 11. Conditions for Use of RESETN

Figure 12. RESETN Minimum Timings

Digital Audio Output Timings

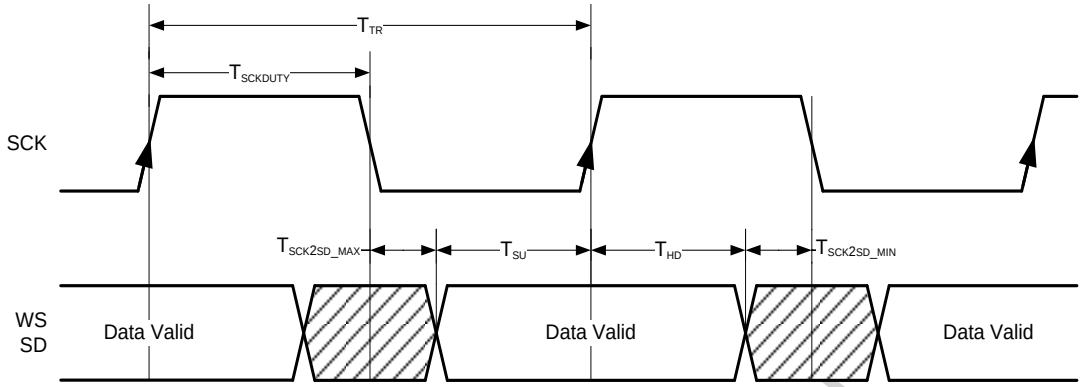


Figure 13. I²S Output Timings

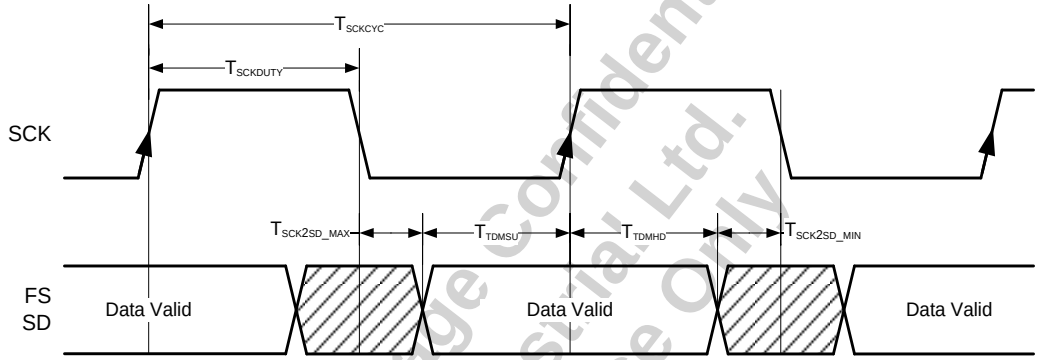


Figure 14. TDM Output Timings

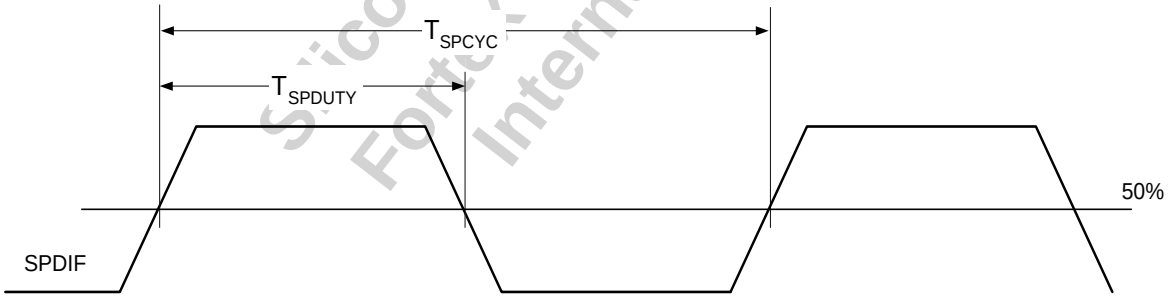


Figure 15. S/PDIF Output Timings

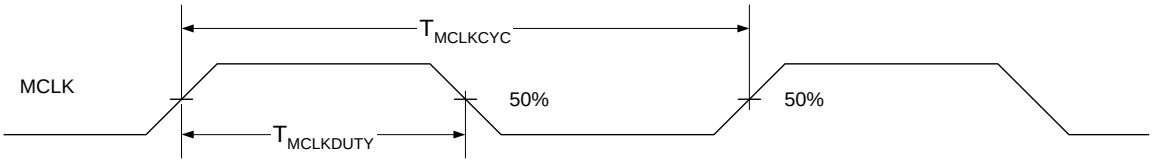


Figure 16. MCLK Timings

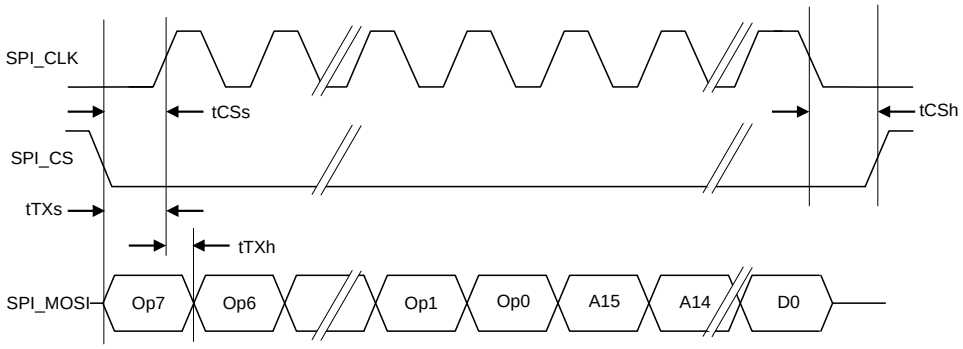


Figure 17. SPI Write Setup and Hold Times

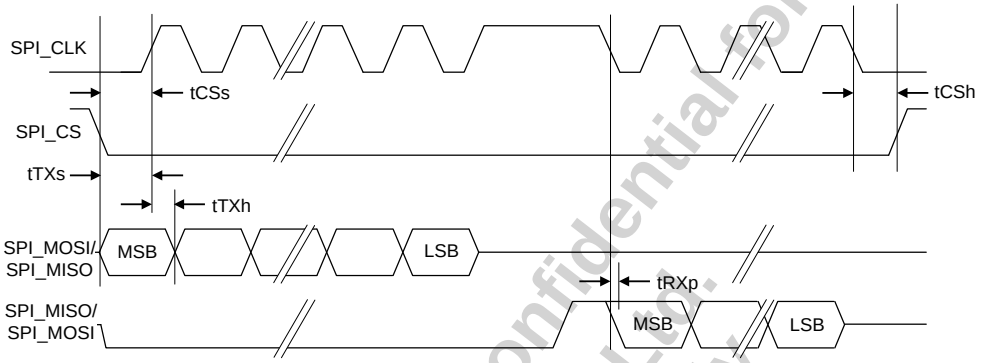


Figure 18. SPI Read Setup and Hold Times

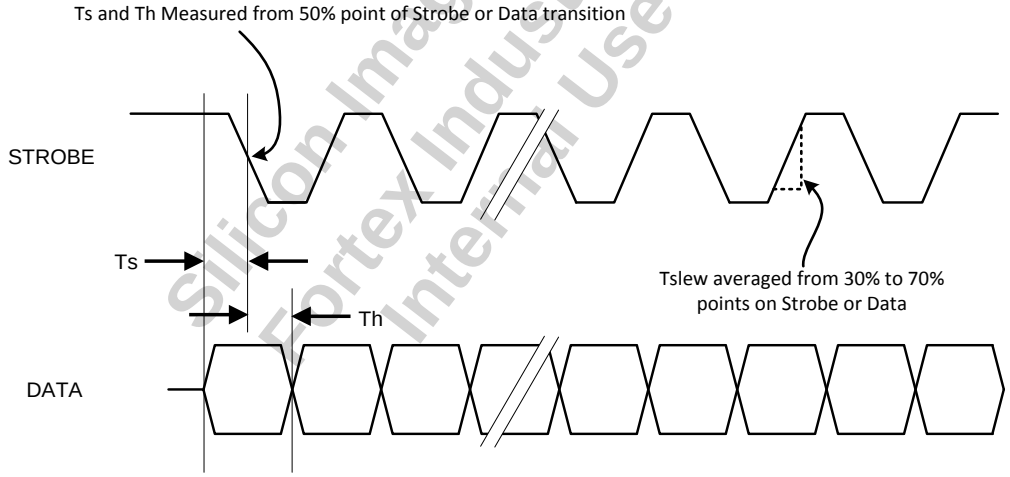


Figure 19. HSIC Timing Diagram

Pin Descriptions

HDMI/MHL1, 2, 3 Receiver Port Pins

Pin Name	Pin	Type	Dir	Description
RXCN	7	TMDS	Input	HDMI Differential Clock Input or Differential Link Clock Input of MHL 3 eCBUS-D mode. In MHL 3 eCBUS-D mode, the differential link clock transmit fixed clock hybrid with SPI/HSIC data and eCBUS commands. In MHL 1.x, MHL 2.x or MHL 3 eCBUS-S mode, this clock pair is not used.
RXCP	8	TMDS	Input	
RX0N	11	TMDS	Input	HDMI Channel 0 Data Input or MHL 1.x, MHL 2.x, and MHL 3 mode Data Input. In MHL 1.x or MHL 2.x mode, this data pair is the single differential pair for a TMDS Data channel carried with common mode clock. The other HDMI channels and clock pair are not used. In MHL 3 mode, this data pair is the single differential pair for a TMDS Data channel without common mode clock. The other HDMI channels and clock pair are not used.
RX0P	12	TMDS	Input	
RX1N	13	TMDS	Input	HDMI Channel 1 Data Input
RX1P	14	TMDS	Input	
RX2N	15	TMDS	Input	HDMI Channel 2 Data Input
RX2P	16	TMDS	Input	
CBUS/CBUS_HPD	4	Custom CBUS 5 V tolerant	Input/ Output	The SiI9394 bridge: CBUS Signal. The SiI9679 receiver: Hot-Plug Detect (HPD) Signal Output for HDMI Mode or CBUS Signal for MHL 1.x, MHL 2.x, and MHL 3 mode. In LPSB mode, if RPWR5V is HIGH and MHL_CD is LOW, this pin will be pulled up HIGH by internal 1 KΩ resistor to wake up function. In normal operation mode, this pin can be controlled by register.
DSCL	75	Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Clock and Data for HDMI Mode. In HDMI mode, these signals are true open-drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor. In MHL 1.x, MHL 2.x or MHL 3 mode, these pins are also used for cable detect input.
DSDA	76	Schmitt Open-drain 5 V tolerant	Input/ Output	

HDMI Transmitter Port Pins

Pin Name	Pin	Type	Dir	Description
TXCN	40	TMDS	Output	HDMI Differential Clock Output.
TXCP	41	TMDS	Output	
TX0N	42	TMDS	Output	HDMI Channel 0 Data Output.
TX0P	43	TMDS	Output	
TX1N	44	TMDS	Output	HDMI Channel 1 Data Output.
TX1P	45	TMDS	Output	
TX2N	46	TMDS	Output	HDMI Channel 2 Data Output.
TX2P	47	TMDS	Output	
TX_HPD	38	5 V tolerant	Input	Hot Plug Detection Input. An external 10 kΩ pull-down resistor is required on this pin.
CEC_A/NC	72	CEC Compliant	Input/ Output	The SiI9394 bridge: Interface to CEC devices. The SiI9679 receiver: NC. For the SiI9394 bridge, this pin is CEC electrical specification compliant signal powered by VDD33. This pin has an internal pull-up. Therefore an external 27 kΩ resistor is not required. For the SiI9679 receiver, this pin must not be connected to anything.
TDSCL	66	Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Clock and Data for transmitter (I^2C Master). These pins implement true open-drain circuits; external pull-up (1.8 kΩ ± 10% typical) resistors to DDC 5 V are required. These are 5 V tolerant pins.
TDSDA	67	Schmitt Open-drain 5 V tolerant	Input/ Output	

Data Tunneling Pins

Pin Name	Pin	Type	Dir	Description
SPI_CLK	60	LVTTL	Input/Output	SPI Master Interface for stand-alone mode and SPI Slave Interface for MHL 3 mode data tunneling function. This interface is shared with the SPI master and slave, only one mode is available at one time. The SPI_CS0 pin is the chip strobe output of the SPI master and should be connected to the external SPI slave device like SPI Flash/EEPROM. And the SPI_CS1 pin is the chip strobe input of the SPI slave and should be connected to the external SPI master device like SoC. This interface defaults to an SPI master and is sampled once at reset to load the data from the external SPI Flash/EEPROM.
SPI_CS0	61	LVTTL	Output	
SPI_CS1	62	LVTTL	Input	
SPI_MOSI	63	LVTTL	Input/Output	
SPI_MISO	64	LVTTL	Input/Output	
HSIC_STB	54	HSIC	Input/Output	HSIC Interface for MHL 3 Mode. In MHL 3 mode, these pins are used to exchange the USB data that transferred over the eCBUS with the external SoC. These pins are not used for other modes.
HSIC_DAT	53	HSIC	Input/Output	

Digital Audio Output Pins

Pin Name	Pin	Type	Dir	Description
XTAL_IN	49	LVTTL	Input	Crystal Clock Input.
XTAL_OUT	50	LVTTL	Output	Crystal Clock Output.
MCLK/NC	29	LVTTL	Output	The SiI9394 bridge: Audio output Master Clock. The SiI9679 receiver: Not Connected (NC)
SCK/NC	28	LVTTL	Output	The SiI9394 bridge: I^2S or TDM Serial Clock. The SiI9679 receiver: NC
WS/NC	27	LVTTL	Output	The SiI9394 bridge: I^2S word select or TDM Frame Start (FS) signal. The SiI9679 receiver: NC
SD0_SPDIF/NC	26	LVTTL	Output	The SiI9394 bridge: I^2S/TDM serial data or S/PDIF audio output. The SiI9679 receiver: NC

Control and Configuration Pins

Pin Name	Pin	Type	Dir	Description
RESETN	34	LVTTL Schmitt	Input	External Reset pin (Active LOW). This pin should not be left floating. An external 4.7 kΩ pull-up resistor to 3.3 V is required.
CSCL	68	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local I^2C Bus Clock. Chip configuration/status registers are accessed through this I^2C port. An external 4.7 kΩ pull-up resistor to 3.3 V is required.
CSDA	69	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local I^2C Bus Data. Chip configuration/status registers are accessed through this I^2C port. An external 4.7 kΩ pull-up resistor to 3.3 V is required.
TMODE	25	LVTTL Schmitt 5 V tolerant	Input	Test Mode Enable. Pull down for normal operation.
INT	20	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Internal MCU Enable Input during POR or Interrupt Output in Normal Operation. This is an open-drain output and requires an external pull-up resistor. During the power-on reset (POR), this pin is used as an input to latch the internal 8051 enabled or not. The level on this pin is latched when the POR transitions from the asserted state to the deasserted state. After completion of POR, this pin is used as interrupt output, which defaults active LOW.
GPIO0_CI2CA	21	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	General Purpose I/O 0 or CI2CA. This pin defaults to an input and is sampled once at reset to select the local I^2C target address ranges.
GPIO1_PSCTL	22	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	General Purpose I/O 1 or PSCTL. In HDMI mode, this pin is used as GPIO 1. In MHL 3 mode, this pin is used as PSCTL to enable or disable system VBUS power to downstream device. This pin defaults to an output.
GPIO2	23	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	General Purpose I/O 2. This pin defaults to an input.
GPIO3	30	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	General Purpose I/O 3. This pin defaults to an input.
GPIO4	31	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	General Purpose I/O 4. This pin defaults to an input.
GPIO5	32	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	General Purpose I/O 5. This pin defaults to an input.
MHL_CD	71	LVTTL Schmitt 5 V tolerant	Input	MHL Cable Detect Input. This pin requires a 300 kΩ pull-down resistor.
WAKEUP	73	LVTTL Open-drain 5 V tolerant	Output	Low Power Standby Mode wakes up pulse output.

Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
XTAL_VDD33	48	Power	XTAL Power.	3.3 V
HSIC_VDD33	57	Power	HSIC Transceiver Power Supply.	3.3 V
VDD33	10	Power	Receiver Termination 3.3 V Analog Power.	3.3 V
VDDIO33	19, 33, 65	Power	Digital I/O Power.	3.3 V
HSIC_VDD10	58	Power	HSIC Analog PHY Interface Power.	1.0 V
VDD10	24, 35, 59, 70	Power	Digital Core Power.	1.0 V
AVDD10_DoC	6	Power	Analog DoC (Data on Clock) Power.	1.0 V
AVDD10	9, 17	Power	Analog Core Power.	1.0 V
AVDD10_PLL	36	Power	Analog PLL Power.	1.0 V
AVDD10_DP	39	Power	Analog Data Path Power.	1.0 V
FVDD10	18	Power	Fractional PLL Power.	1.0 V
MVDD10/NC	52	Power	The SiI9394 bridge: Audio PLL Power. The SiI9679 receiver: NC	1.0 V
VDD5V_IN	2	Power	Local Power 5 V Input. If there is no RPWR5V input, an active 5 V power input of this pin is required.	5 V
LPSBV	74	Power	Standby Power for Low Power Standby Mode.	5 V
RPWR5V	3	Power	5 V Port Detection Input. Connect to 5 V signal from HDMI input connector. This pin requires a 10 Ω series resistor, a 5.1 kΩ pull-down resistor, and at least a 1 µF capacitor to ground.	5 V
VDD33OUT	1	Power	Internal 3.3 V Regulator Output. This pin requires a 4.7 µF capacitor to ground. Must not be used as any external power supply.	—
VDD12OUT	56	Power	Internal 1.2 V Regulator Output. This pin requires a 4.7 µF capacitor to ground. Must not be used as any external power supply.	—
CoC_GND	5	Ground	Clock over CBUS Ground. This pin must be connected to Ground.	Ground
XTAL_GND	51	Ground	XTAL Ground.	Ground
HSIC_GND	55	Ground	HSIC Interface Ground.	Ground
GND	ePad	Ground	Ground. All ground connections to the device are through the ePad, therefore it must be soldered to the board and the pad must have a low resistance connection to the board ground plane.	Ground

Not Connected Pins for the SiI9679 Bridge

Name	Pin	Type	Description
NC	37, 73	NC	Not Connected. These pins must not be connected to anything.

Not Connected Pins for the SiI9679 Receiver

Name	Pin	Type	Description
NC	26, 27, 28, 29, 37, 52, 72	NC	Not Connected. These pins must not be connected to anything.

Feature Information

RGB to YCbCr Color Space Converter

The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr formats. Table 27 shows the conversion formulas that are used. The HDMI AVI packet defines the color space of the incoming video.

Table 27. RGB to YCbCr Conversion Formulas

Video Format	Conversion	Formulas
		CE Mode 16-235 RGB
VGA	ITU-R BT.601	Y = 0.299R′ + 0.587G′ + 0.114B′ Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
WVGA	ITU-R BT.601	
SVGA	ITU-R BT.601	
480p/i	ITU-R BT.601	
576p/i	ITU-R BT.601	
XGA	ITU-R BT.709	Y = 0.213R′ + 0.715G′ + 0.072B′ Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
SXGA	ITU-R BT.709	
UXGA	ITU-R BT.709	
WUXGA	ITU-R BT.709	
720p	ITU-R BT.709	
1080i	ITU-R BT.709	
1080p	ITU-R BT.709	
4K x 2K	ITU-R BT.709	

YCbCr to RGB Color Space Converter

The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. See Table 28 for the detailed formulas. Note the difference between RGB range for CE modes and PC modes.

Table 28. YCbCr-to-RGB Conversion Formulas

Format Change	Conversion	YCbCr Input Color Range
YCbCr 16-235 Input to RGB 16-235 Output	601*	R′ = Y + 1.371(Cr – 128) G′ = Y – 0.698(Cr – 128) – 0.336(Cb – 128) B′ = Y + 1.732(Cb – 128)
	709	R′ = Y + 1.540(Cr – 128) G′ = Y – 0.459(Cr – 128) – 0.183(Cb – 128) B′ = Y + 1.816(Cb – 128)
YCbCr 16-235 Input to RGB 0-255 Output	601	R′ = 1.164((Y-16) + 1.371(Cr – 128)) G′ = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B′ = 1.164((Y-16) + 1.732(Cb – 128))
	709	R′ = 1.164((Y-16) + 1.540(Cr – 128)) G′ = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B′ = 1.164((Y-16) + 1.816(Cb – 128))

***Note:** No clipping can be done.

SiI9394 and SiI9679 Input and Output Matrix with HDCP

The SiI9394 bridge and the SiI9679 receiver support different HDCP modes. See Table 29 below for details.

Table 29. SiI9394 and SiI9679 Input and Output Matrix with HDCP

Device	HDCP Mode	Input				Output
		HDMI	MHL 1.x/MHL 2.x	MHL 3 (eCBUS-S)	MHL 3 (eCBUS-D)	HDMI
SiI9394 Bridge	HDCP 1.x	—	Y	Y	Y	Y[2]
	HDCP 2.2	—	N	Y	Y	Y[2]
SiI9679 Receiver	HDCP 1.x	Y	Y	Y	Y	Y[3]
	HDCP 2.2	Y	N	Y	Y	N

Notes:

1. Y = Supported, N = Not Supported.
2. The SiI9394 bridge supports three types of HDCP repeater: HDCP 2.2 repeater, HDCP 1.x repeater, HDCP 2.2 to HDCP 1.x down-converter.
3. The SiI9679 receiver supports HDMI output without HDCP, and supports optional HDCP 1.x output only for HDCP 2.2 input without repeater function.

3D Video Formats

The SiI9394 or the SiI9679 device supports the 3D video modes described in the HDMI 1.4a Specification. All modes support RGB 4:4:4, YCbCr 4:2:2 and YCbCr 4:4:4 color formats and 8-bit color depth. External separate HSYNC, VSYNC, and DE signals can be supplied, or these signals can be supplied as embedded EAV/SAV sequences in the video stream. Table 30 shows only the maximum possible resolution with a given frame rate. For example, Side-by-Side mode is defined for 1080p @ 60 Hz frame, which implies that 720p @ 60 Hz and 480p @ 60 Hz are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported. A frame rate of 60 Hz means a frame rate of 59.94 Hz and its associated pixel frequency is supported as well.

Table 30. Supported HDMI 3D Input Video Formats

HDMI 3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	
Side-by-Side	Full	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	
	Half	1080p	50/60	
Top-and-Bottom	—	1080p	50/60	74.25
		1080p	24/30	
		720p/1080i	50/60	
Line Alternative	—	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	
Field Alternative	—	1080i	50/60	
L + Depth	—	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	

When the SiI9394 or the SiI9679 device is in MHL 2.x, MHL 3 eCBUS-S mode, or MHL 3 eCBUS-D mode, the MHL 3D input formats are transcoded to HDMI mode 3D formats accordingly. The supported MHL input 3D formats are listed in Table 31, Table 32, and Table 33.

Table 31. Supported MHL 3 (eCBUS-D) Mode 3D Input Video Formats

MHL 3 (eCBUS-D) Mode 3D Format	Corresponding HDMI Format	Resolution	Frame Rate (Hz)	Input Pixel Clock for 8-bit color (MHz)
Frame Sequential	Frame Packing	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	
Top-Bottom	Top-and-Bottom	1080p	50/60	148.5
		1080p	24/30	74.25
		720p/1080i	50/60	
Left-Right	Side-by-Side (Half)	1080p	50/60	148.5
		1080p	24/30	74.25
		720p/1080i	50/60	74.25

Table 32. Supported MHL 3 (eCBUS-S) Mode 3D Input Video Formats

MHL 3 (eCBUS-S) Mode 3D Format	Corresponding HDMI Format	Resolution	Frame Rate (Hz)	Input Pixel Clock for 8-bit color (MHz)
Frame Sequential	Frame Packing	1080p	50/60	300 (PackedPixel)
		1080p	24/30	148.5
		720p/1080i	50/60	
Top-Bottom	Top-and-Bottom	1080p	50/60	148.5
		1080p	24/30	74.25
		720p/1080i	50/60	
Left-Right	Side-by-Side (Half)	1080p	50/60	148.5
		1080p	24/30	74.25
		720p/1080i	50/60	74.25

Table 33. Supported MHL 2 3D Input Video Formats

MHL 2 3D Format	Corresponding HDMI Format	Resolution	Frame Rate (Hz)	Input Link Clock for 8-bit color (MHz)
Frame Sequential	Frame Packing	1080p	24/30	74.25 (PackedPixel)
		720p/1080i	50/60	
Top-Bottom	Top-and-Bottom	1080p	50/60	74.25 (PackedPixel)
		1080p	24/30	74.25
		720p/1080i	50/60	
Left-Right	Side-by-Side (Half)	1080p	50/60	74.25 (PackedPixel)
		1080p	24/30	74.25
		720p/1080i	50/60	74.25

Device Address Configuration Using CI2CA/GPIO4/GPIO5

All functions of the SiI9394 or the SiI9679 device are controlled and observed with I^2C registers. The I^2C address of the device depends on the working mode: External MCU mode or stand-alone mode. The GPIO0_CI2CA/GPIO4/GPIO5 pins default to an input signal and are sampled once at reset to select the local I^2C address ranges.

For External MCU mode, CI2CA signal is used for the local I^2C address selection, which is fixed to 0x60/0x62. Refer to Table 34.

Table 34. Control of I2C Address with CI2CA Signal

Local I^2C address of Page 0	CI2CA
0x60	Low
0x62	High

For stand-alone mode GPIO4 and GPIO5 signals are used for the local I^2C address selection, which is defined by the firmware of internal MCU. Refer to the Table 35.

Table 35. Control of I2C Address with GPIO4/GPIO5 Signal

Local I^2C address of Page 0	GPIO4	GPIO5	Notes
Value1	Low	Low	1, 2
Value2	Low	High	1, 2
Value3	High	Low	1, 2
Value4	High	High	1, 2

Notes:
1. The I2C address value is defined by firmware of the internal MCU.
2. Value1, 2, 3, and 4 is configurable based on system design requirement.

Audio Output Interface

S/PDIF

The S/PDIF stream can carry two-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data output logic forms the audio data output stream from the HDMI audio packets. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes. Coherent means that the MCLK and S/PDIF are created from the same clock source.

I^2S

The I^2S bus format is programmable through registers, to allow interfacing with I^2S audio DACs or audio DSPs with I^2S inputs. Additionally, the MCLK (audio master clock) frequency is selectable to be an integer multiple of the audio sample rate Fs.

MCLK frequencies support various audio sample rates as shown in Table 36.

Table 36. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs : I^2S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	—	—
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz	—	—

TDM

Serial audio interfaces such as I²S and TDM consist of words and channels (or slots), as shown in Figure 20.

HDMI and MHL allow 24-bit words. The TDM allows 32-bit channels. Each channel has up to 24-bit audio word and zero pads for the rest. The TDM frame can have 2/4/6/8 channel. TDM FS (Frame Start) identifies the first channel of the TDM frame, as shown in Figure 21.

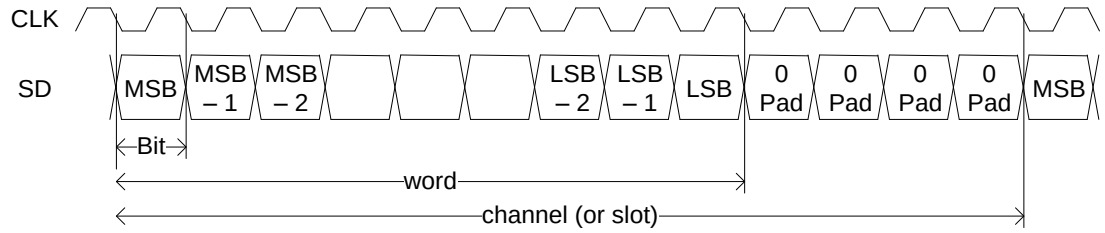


Figure 20. Word and Channel in TDM Audio Interface

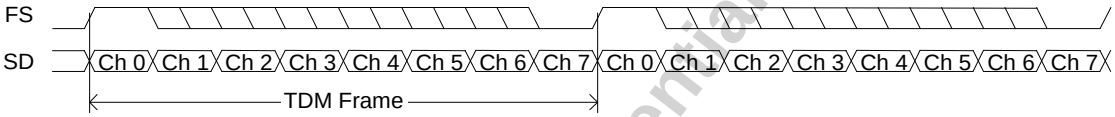


Figure 21. TDM Frame

In TDM, the first channel MSB has a one bit delay to FS. To cover the compliance issues, we have three options between the MSB of the first channel and FS: No delay, 1-bit delay, or 2-bit delay, as shown in Figure 22.

The control registers of the TDM share I²S.

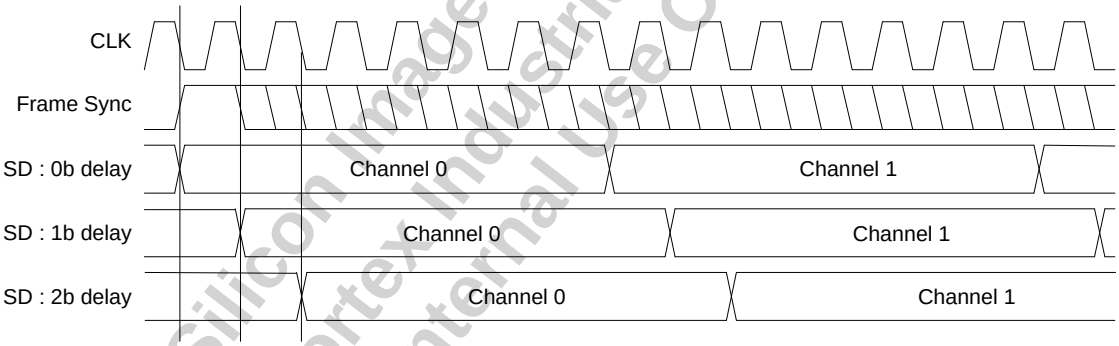


Figure 22. TDM – Delay of First Channel MSB to FS

AV Link Data Rate in MHL 3 Mode

When the SiI9394 or the SiI9679 device operates in MHL 3 mode, Receiver Block of the AV Link stream can be configured to 6Gbps, 3Gbps, and 1.5Gbps data rate, which depends on the setting of CBUS command - AV LINK_MODE_CONTROL from the MHL 3 source.

The capability of the Receiver Block varies depending on its setting for a different TMDS link data rate mode. MHL 3 source should carefully select the link rate based on pixel clock of the video format, power consumption, and EMI requirement.

Table 37 shows bandwidth limitations of the input video pixel clock under different data rate.

Table 37. Input Video Pixel Clock Bandwidth vs. AV link Data Rate in MHL 3 Mode

eCBUS Mode	Link Clock Frequency	Video Format Color Depth	AV Link Data Rate	Input Video Pixel Clock Bandwidth
eCBUS-S	75 MHz	16bpp (YCbCr 4:2:2, Packet Pixel mode)	1.5 Gbp/s	Up to 75 MHz
			3.0 Gbp/s	Up to 150 MHz
			6.0 Gbp/s	Up to 300 MHz
		24bpp (YCbCr 4:4:4 or RGB)	1.5 Gbp/s	Up to 50 MHz
			3.0 Gbp/s	Up to 100 MHz
			6.0 Gbp/s	Up to 200 MHz
eCBUS-D	150 MHz	16bpp (YCbCr 4:2:2, Packet Pixel mode)	1.5 Gbp/s	Up to 75 MHz
			3.0 Gbp/s	Up to 150 MHz
			6.0 Gbp/s	Up to 300 MHz
		24bpp (YCbCr 4:4:4 or RGB)	1.5 Gbp/s	Up to 50 MHz
			3.0 Gbp/s	Up to 100 MHz
			6.0 Gbp/s	Up to 200 MHz

Design Recommendations

The tolerance of all resistors shown in this section is ± 5% unless otherwise noted.

Power Supplies Decoupling

Silicon Image recommends that designers include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 23. Place these components as close as possible to the pins of the SiI9394 or the SiI9679 device, and avoid routing traces through vias if possible. An example of this layout configuration is shown in Figure 24. Connections in one group (such as VDD) can share C2, the ferrite, and C3, with each pin having a separate C1 placed as close to the pin as possible. Suggested values for C1, C2, and C3 are 0.01 µF, 0.1 µF, and 10 µF, respectively. The recommended impedance of ferrite L1 is 10 Ω or more in the frequency range of 1 – 2 MHz for all power supplies.

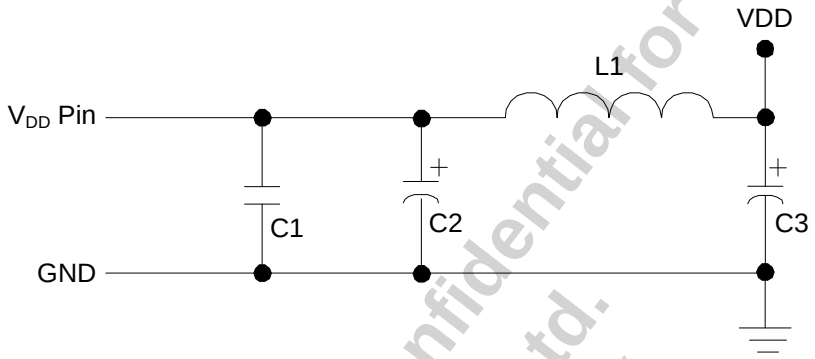


Figure 23. Decoupling and Bypass Schematic

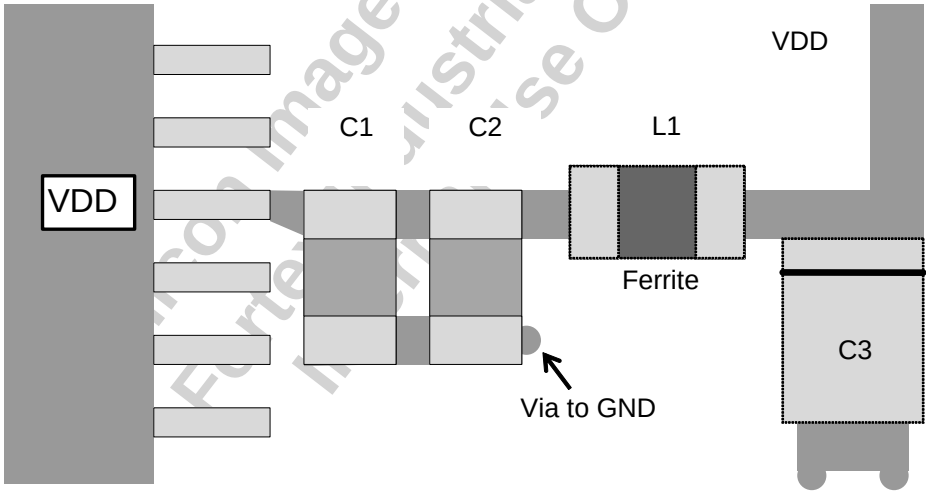


Figure 24. Decoupling and Bypass Capacitor Placement

High-speed TMDS Signals

Layout Guidelines

The layout guidelines below help to ensure signal integrity. Silicon Image strongly encourages the board designer to follow these guidelines.

- Place the input and output connectors that carry the TMDS signals as close as possible to the device.
- Route the differential lines as directly as possible from the connector to the device when using industry-standard HDMI connectors.
- Route the two traces of each differential pair together.
- Minimize the number of vias through which the signal lines are routed.
- Lay out the MHL input pin traces with a controlled differential impedance of 100 Ω and a common mode impedance of 30 Ω. The differential impedance of the HDMI output pins must be designed within ± 15% of 100 Ω.
- Serpentine traces are not recommended to compensate for inter-pair trace skew.
- Lay out the HSIC trace with a controlled impedance of 50 Ω within ± 10% range. Circuit board trace length should be less than 10 cm.

ESD Protection

The SiI9394 or the SiI9679 device can withstand electrostatic discharges (ESD) due to handling during manufacture. In applications where higher protection levels are required, ESD-limiting components can be placed on the differential lines of the chip. These components typically have a capacitive effect that reduces the signal quality at higher clock frequencies. Use the lowest capacitance devices possible. ESD components must be placed after the receiver series termination resistors and as close as possible to the input or output connector. In no case can the capacitance value of these components exceed 1 pF.

EMI Considerations

Electromagnetic interference (EMI) is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines, except the common-mode chokes and ESD protection described earlier. The differential signaling used in HDMI is inherently low in EMI if the routing recommendations noted in the Layout Guidelines section are followed.

The PCB ground plane should extend unbroken under as much of the transmitter chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

Packaging

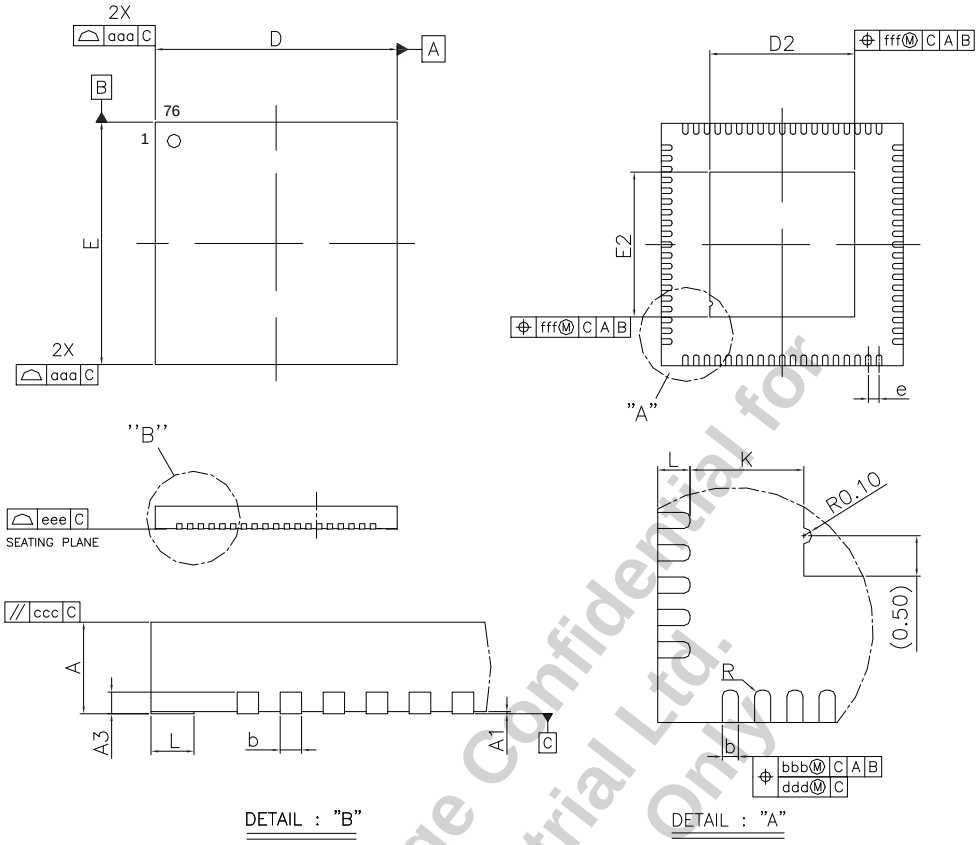
ePad Requirements

The SiI9394 or the SiI9679 chip is packaged in a 76-pin, 9 mm × 9 mm QFN package with an ePad that is used for electrical ground of the device and for improving thermal transfer characteristics.

The ePad dimensions are 5.38 mm × 5.38 mm shown on the following page. Soldering the ePad to the ground plane of the PCB is ***required*** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. As a general guideline, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical short circuit. Figure 25 on page 44 shows the package dimensions of the SiI9394 or the SiI9679 device.

Package Dimensions

Package drawings are not to scale.



JEDEC Package Code MO-220

Symbol	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A1	Stand-off	0.00	0.02	0.05
A_3	Base thickness		0.20 REF	
D / E	Body size	8.90	9.00	9.10
D2 / E2	ePad size	6.15	6.30	6.45
b	Plated lead width	0.15	0.20	0.25
e	Lead pitch		0.40 BSC	
L	Lead foot length	0.30	0.40	0.50
R	Lead tip radius	0.075	—	—
K	Lead to ePad clearance	0.20	—	—
aaa	—		0.10	
bbb	—		0.07	
ccc	—		0.10	
ddd	—		0.05	
eee	—		0.08	
fff	—		0.10	

All dimensions are in millimeters.

Figure 25. 76-pin QFN Package Diagram

Marking Specification

Marking drawing is not to scale.

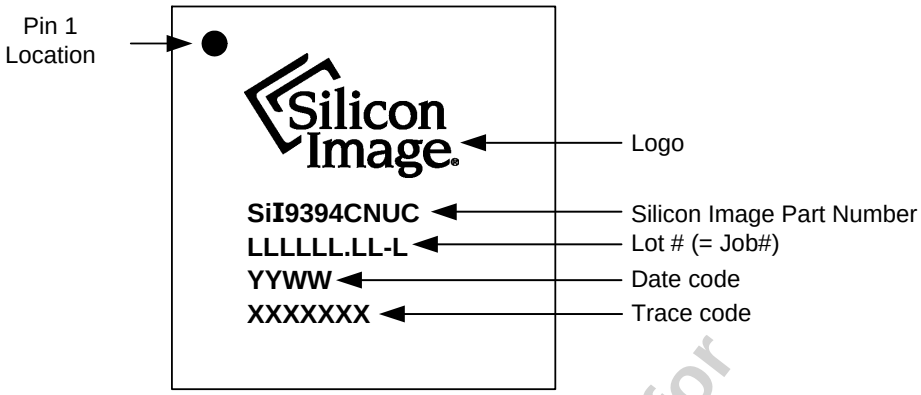


Figure 26. Marking Diagram for SiI9394 Bridge

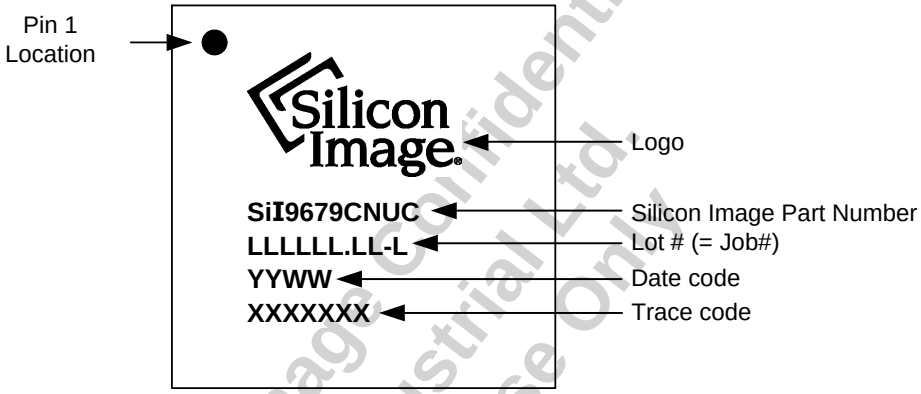


Figure 27. Marking Diagram for SiI9679 Receiver

Ordering Information

Production Part Numbers:

Part Number	Device
SiI9394 CNUC	SiI9394 MHL 1, 2, 3 to HDMI Bridge with HDCP 2.2 Support
SiI9679 CNUC	SiI9679 HDMI/MHL 1, 2, 3 Receiver with HDCP 2.2 Support

The universal package can be used in lead-free and ordinary process lines.

References

Standards Documents

Table 38 lists the abbreviations used in this document. Contact the responsible standards groups listed in Table 39 for more information on these specifications.

Table 38. Referenced Documents

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface, Revision 1.4a,* HDMI Consortium, March 2010
HCTS	*HDMI Compliance Test Specification, Revision 1.4a,* HDMI Consortium, March 2010
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, March 2001
CEA-861-D	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, Draft 020328, EIA/CEA; July 2006
EDDC	*Enhanced Display Data Channel Standard, Version 1.1,* VESA; March 2004
I^2C	*The I^2C Bus Specification,* Version 2.1, Philips Semiconductors, January 2000
MHL	*MHL (Mobile High-definition Link) Specification,* Version 3, MHL, LLC, Month 2013

Table 39. Standards Groups Contact Information

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
I^2C	http://www.nxp.com	—	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—
MHL	http://www.mhlconsortium.org	Customerservice@mhlconsortium.org	408-962-4269

Silicon Image Documents

Table 40 lists Silicon Image documents that are available from your Silicon Image sales representative.

Table 40. Silicon Image Publications

Document	Title
SiI-AR-1000	*SiI9394 Software API Reference Document*

Revision History

Revision B, February 2014

Summary of additions and changes:

- Table 4. DC Digital I/O Specifications, updated $V_{OH,}$ V_{OL} and V_{OL_DDC} Conditions; updated $V_{OL\_DDC.}$ Parameter.
- Table 9. Digital CBUS I/O Specifications, specified Min value for V_{OH_CBUS}.
- Table 14. TMDS Input Timings – HDMI Mode, specified Max value for F_{RXC}.
- Updated Table 15. TMDS Input Timings – MHL 1/MHL 2 Mode, Table 16. TMDS Input Timings – MHL 3 (eCBUS-S) Mode, and Table 17. TMDS Input Timings – MHL 3 (eCBUS-D) Mode.
- Table 26. ESD Specifications, updated value for HBM, MM, and CDM.

Revision A, January 2014

First production release.

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