SiI8784 Multi-format Analog Video Front-end with HDMI/MHL Transmitter

Data Sheet

SiI-DS-1122-C

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1. General Description

The Lattice Semiconductor SiI8784 device is a high quality, multi-format analog video decoder and processor with an integrated dual-mode High Definition Multimedia Interface (HDMI®)/Mobil High-definition Link (MHL®) transmitter. A microcontroller is integrated to reduce the system Bill Of Materials (BOM) cost.

The SiI8784 device supports worldwide PAL, NTSC and SECAM standards, YPbPr video signals up to 1080p @ 60 Hz resolution, and RGB graphics signals from VGA to UXGA resolutions. It also supports the SCART interface with Fast Blanking and the D-Terminal.

This device contains a Time Base Correction (TBC) module, a de-interlacer with a post-processor engine, and a VBI decoder. For content protected analog videos, HDCP will automatically be enabled on the HDMI or MHL output.

1.1. Features

1.1.1. Analog Video Front-end

- Four 10-bit Analog to Digital Convertors (ADC) sampling up to 170 MHz
- Flexible input multiplexers to support composite, component, VGA, SCART with Fast Blanking and D-Terminal interfaces
- Supports cable plug-in detection and active video signal detection

1.1.2. Multi-format Video Decoder

- Automatic format detection
- Supports NTSC, PAL, and SECAM standards of composite input with adaptive comb filter
- Supports 240p, 480i/p, 576i/p, 720p, 1080i/p component video
- Supports RGB graphics from VGA to UXGA
- Supports Macrovision Type I, II, III copy protection detection
- Supports multi-standard VBI decoding: Teletext, WSS, VPS, CC, CGMS, and V-CHIP

1.1.3. Video Processing

- Time Base Correction
- De-interlacer with Edge Smoothing
- Automatic Phase/Position Detection

1.1.4. HDMI/MHL Transmitter

- Selectable HDMI/MHL Dual-mode
- Compliant with HDMI 1.4b and MHL 2.1 specifications
- HDMI output up to 1080p @ 60 Hz or UXGA @ 60 Hz resolution
- MHL output up to 1080p @ 60 Hz resolution
- HDCP 1.4
- Audio insertion with I^2S/ SPDIF input
- VBI data forwarding over HDMI/MHL

1.2. Applications

The SiI8784 device is targeted for the Digital TV (DTV) market.

1.3. Packaging

- 88-pin QFN with exposed pad (ePad)
- 10 mm × 10 mm × 0.9 mm

1.4. Temperature Range

- 0 °C to +70 °C

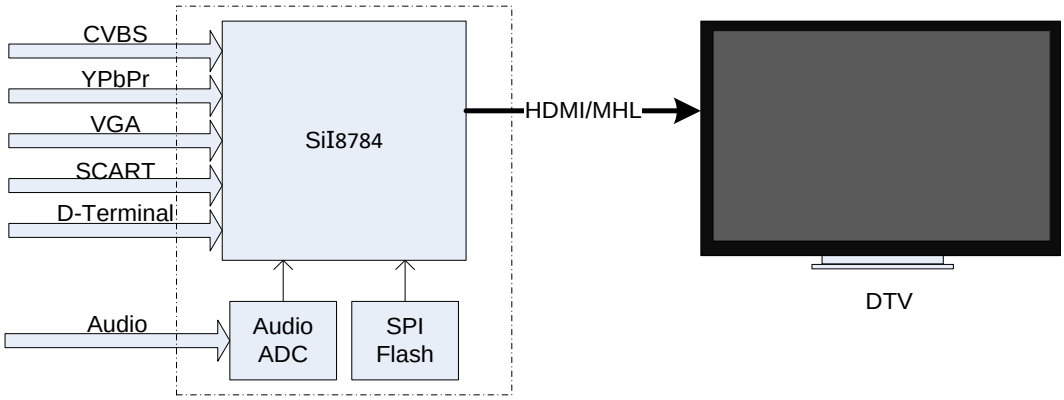


Figure 1.1. Typical Application of the SiI8784 Device

2. Product Family

A comparison of the features between the SiI8784 device and the SiI8788 device is shown in Table 2.1.

Table 2.1. Product Selection Guide

Feature	SiI8784	SiI8788
Analog Video Input		
Component (YP_bP_r)	YES	YES
Composite (CVBS)	YES	YES
D-Terminal	YES	NO
RGB graphics (VGA)	YES	NO
SCART with Fast Blanking	YES	NO
Digital Video Output		
Parallel	NO	YES
HDMI	YES	NO
MHL	YES	NO
Audio Input		
SPDIF Input	YES	NO
I^2S Input	YES	NO
Package		
Package Type	QFN	QFN
Pin Count	88	88

3. Functional Description

The SiI8784 device has four subblocks in its signal path and one control block: Analog Front-end (AFE), Video Decoder (VDC), Video Processing, HDMI/MHL transmitter and Control Logic. Figure 3.1 shows the block diagram.

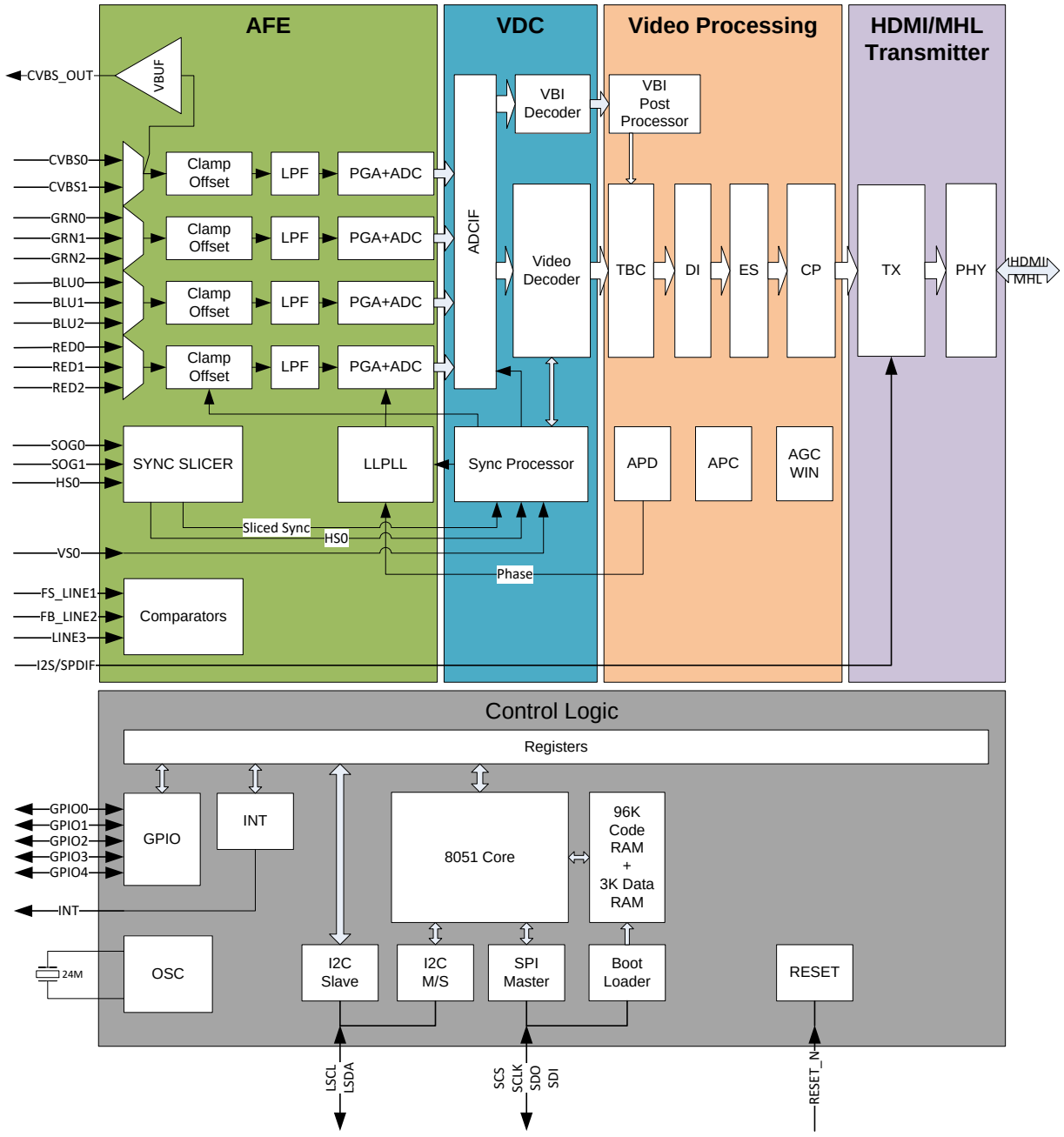


Figure 3.1. Functional Block Diagram

Each subblock is described in the following sections.

3.1. Analog Front-end

The Analog Front-end (AFE) provides four input channels for CVBS, R, G, and B. Each channel includes an Input Multiplexer, a Clamp and Offset DAC, a Programmable Low-pass Filter, and a high quality 10-bit ADC with Programmable Gain Amplifier. In addition, there is a Line Locked PLL to generate sampling clocks for ADCs, Sync Slicers to handle SOG signals, a set of input comparators to support SCART and D-terminal interfaces, and a CVBS output buffer to support SCART.

3.1.1. Input Multiplexer

The SiI8784 device provides two CVBS inputs, and three R/G/B inputs for flexible configurations. Table 3.1 and Table 3.2 show some examples.

Table 3.1. Inputs Configuration with SCART Interface

—	CVBS0	CVBS1	RED0	RED1	RED2	GRN0	GRN1	GRN2	BLU0	BLU1	BLU2
CVBS	CVBS	—	—	—	—	—	—	—	—	—	—
Component	—	—	—	P_r	—	—	Y	—	—	Pb	—
VGA	—	—	—	—	R	—	—	G	—	—	B
SCART	—	CVBS	R	—	—	G	—	—	B	—	—

Table 3.2. Inputs Configuration with D-Terminal Interface

—	CVBS0	CVBS1	RED0	RED1	RED2	GRN0	GRN1	GRN2	BLU0	BLU1	BLU2
CVBS	CVBS	—	—	—	—	—	—	—	—	—	—
Component	—	—	—	P_r	—	—	Y	—	—	Pb	—
VGA	—	—	—	—	R	—	—	G	—	—	B
D-Terminal	—	—	Pr	—	—	Y	—	—	Pb	—	—

3.1.2. Clamp and Offset

As most of the video signals, such as CVBS, are AC coupled, their DC component is lost during the transmission. A voltage type clamp circuit is positioned in front of each channel to restore the DC component.

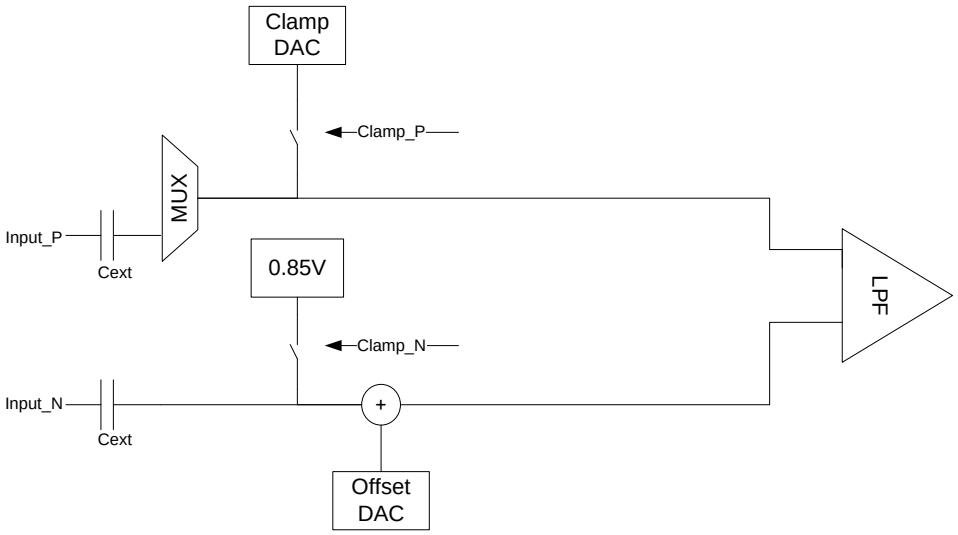


Figure 3.2. Clamp and Offset

The clamp DAC output voltage is 3-bit programmable and AFE provides more accurate 10-bit ±0.5 V output offset DAC to keep the input signal within the ADC input range. The offset level can be controlled automatically by ADCIF block of VDC or manually by software.

3.1.3. Low-pass Filter

The Low-pass Filter (LPF) is a first order analog filter to remove the out-of-band noise from video signal. Its –3 dB bandwidth can be set to 600 MHz (Bypass), 400 MHz, 200 MHz, 100 MHz, or 50 MHz by software. Combined together with ADC over-sampling technology and the high order digital AA (Anti-alias) filter inside VDC, the SiI8784 device can meet the demand of overall AA performance.

3.1.4. ADC with Programmable Gain Amplifier

The ADC samples the input video signal and converts each sample into 10 bits digital data. It supports the sampling rates from 25 MSPS to 170 MSPS, and the sampling clock of CVBS channel can be independent with R, G, and B channels.

For the formats with lower pixel rate, oversampling is recommended. The SiI8784 device supports 2X, 4X and 8X oversampling.

The Programmable Gain Amplifier (PGA) in the front stage of ADC has a nominal gain range from –6 dB to +6 dB, so the SiI8784 device can adapt to a wide range of input video signal levels, especially the CVBS signal from an RF tuner. The PGA can be controlled either automatically by the gain control function of VDC or manually by software.

3.1.5. Line Locked PLL (LLPLL)

The Line Locked PLL (LLPLL) is designed to generate the ADC sampling clock, i.e. pixel clock or oversampled pixel clock. It can be synchronized with a slower reference HSync pulses or run at a fixed frequency. The allowable input HSync range is from 15 kHz to 150 kHz, and the output pixel clock range is from 25 MHz to 170 MHz.

The LLPLL contains a high performance programmable digital PLL (DPLL) and an analog PLL (APLL) which generates the high frequency reference clock needed by the DPLL from the 24 MHz crystal frequency.

The relative phase between the input sync pulse and the output clock of LLPLL can be adjusted in 32 steps by setting registers or automatically by the Auto Phase Detection (APD) block of the video processing module.

3.1.6. Sync Slicer

The Sync Slicer converts SOG and HSYNC signals into core domain digital signals. As shown in Figure 3.3, there are two sets of SOG slicers, each of contains an input multiplexer, a bottom level (0.5 V) clamp, a low pass filter, and a comparator. The comparator threshold is programmable. Also, there are two sets of HS slicers for TTL level syncs. When one of the slicers is configured as an active input, the other can be used to detect the activity of other inputs. This feature is helpful to implement the active channel detection and auto-switch functions.

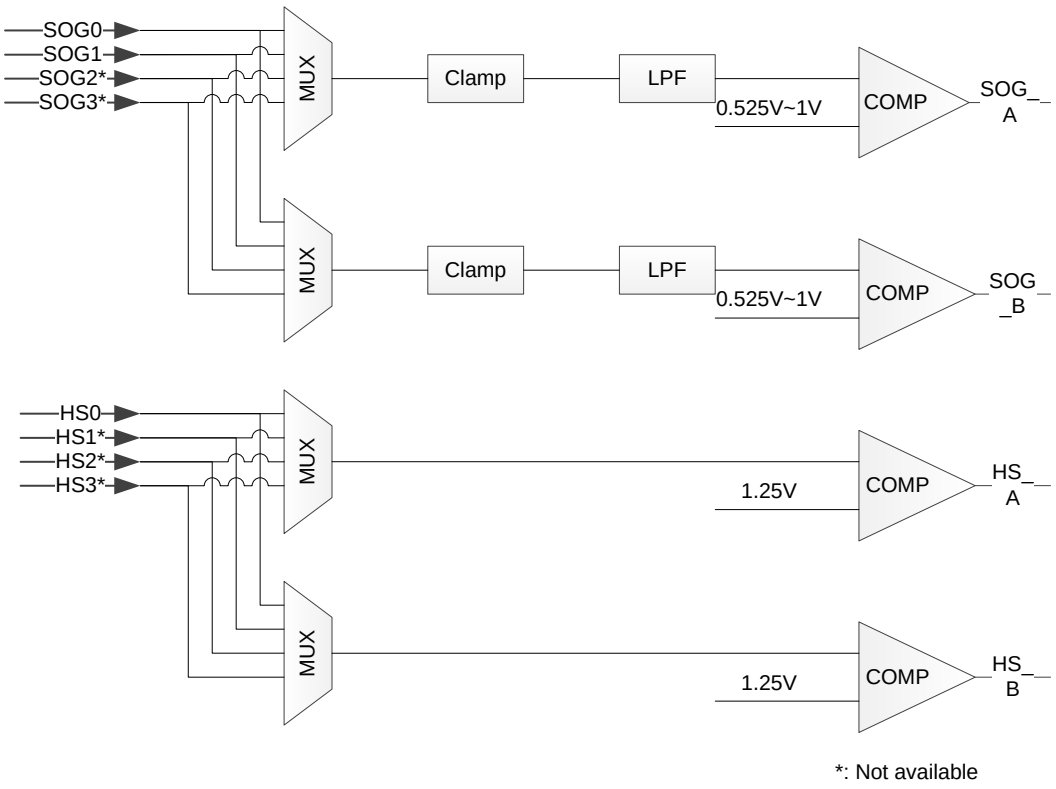


Figure 3.3. Sync Slicers

3.1.7. Video Buffer (VBUF)

The Video Buffer (VBUF) buffers and outputs the selected CVBS input signal. This feature is useful to implement the CVBS return channel of the SCART interface. VBUF includes two major subblocks: clamp and voltage-to-current conversion. The Voltage-to-current conversion subblock converts the input signal to the output current which is proportional to the signal voltage level. A 75 Ω source termination resistor should be connected to the CVBS_OUT output pin and signal ground.

3.2. Video Decoder (VDC)

The SiI8784 device provides a multi-format video decoder. VDC includes ADCIF, Sync Processor, adaptive 2D Comb decoder, and VBI Decoder blocks as shown in Figure 3.1 on page 7.

3.2.1. ADCIF

The ADCIF logic block contains Automatic Gain Control and Offset Calibration, and Anti-alias filtering and decimation subblocks. It also generates clamp pulses for clamp circuits at the proper time so that ADC is able to digitize the input analog within the proper range. The main indicator used to determine where the clamping position should be is the horizontal synchronization pulse coming from the Sync Processor block. Since this filtered HSync pulse may not always be correct, several layers of logic have been developed to ensure the clamping is not done at an incorrect position.

3.2.1.1. Automatic Gain Control and Offset Calibration

Parameters such as Sync Amplitude, Back Porch Levels are measured based on the HSync position, register controls, and logic executed in the Offset Gain Calculations sub block. These measured values are then used in determining the offset and gain adjustments. To ensure the stability and accuracy of digitized video signal, several control loops are built in the ADCIF block. These loops include Clamp, Coast, Gain, and Offset. The Clamp and Coast pulses, Gain and Offset parameters are generated by the ADCIF logic and directly connected to the AFE.

3.2.1.2. Anti-alias Filtering and Decimation

The Anti-aliasing (AA) filters remove high frequency noise from the raw digitized signals produced by the front-end video ADCs, and decimate the over-sampled video signal.

The AA filter has flexibility in the frequency response, sharp transition bandwidth, and good stop band attenuation. The AA filter allows the software to change the bandwidth of the filters as the signal conditions changes.

3.2.1.3. Video Decoder

Video Decoder block processes both CVBS data stream and component/RGB data stream. It also supports the SCART Fast Blanking functions.

3.2.1.4. CVBS Processing

CVBS Processing involves the Standard Detection, 2D Video Decoder, and Sync Processor subblocks, as shown in Figure 3.4 below.

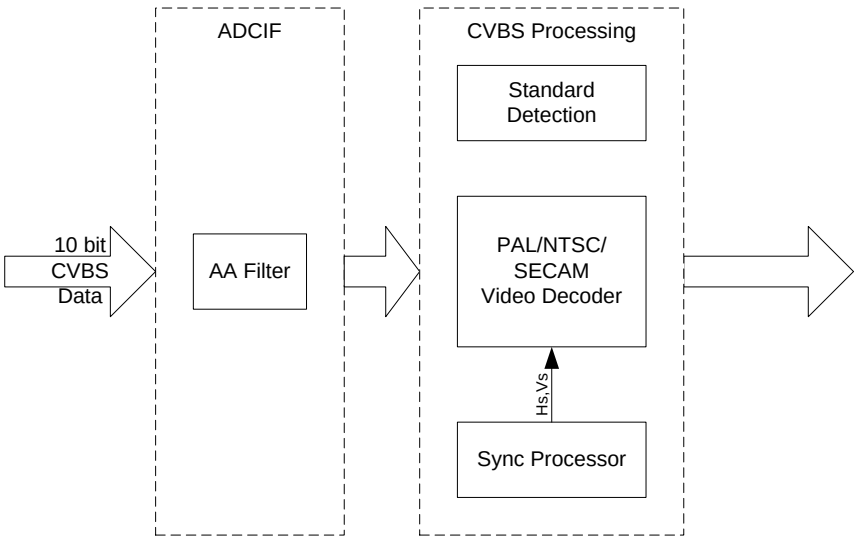


Figure 3.4. CVBS Processing Diagram

The SiI8784 device can automatically detect NTSC (M/J/4.43), PAL (B/D/I/G/H/60/M/N/Nc), and SECAM (B/D/G/L/K) standards, and decode them properly.

An adaptive 2D comb filter is used in video decoder. The 2D comb filter has three output options, only horizontal filter, only vertical filter and blending of horizontal and vertical filter. When the current sample is on a horizontal transition edge, the vertical filter is selected. When the current sample is on a vertical transition edge, the horizontal filter is selected. When it is not one of the above two phenomenon, the blending output is selected.

When the input signal is lost, the SiI8784 device can operate in a free-running mode to ensure a stable output.

3.2.1.5. Component/RGB Processing

Component/RGB Processing processes Component Video and RGB Graphics. Component Video Processing includes Sync Processor. Figure 3.5 shows the block diagram of the component video and RGB Graphics processing. The following sections explain each of the blocks in detail.

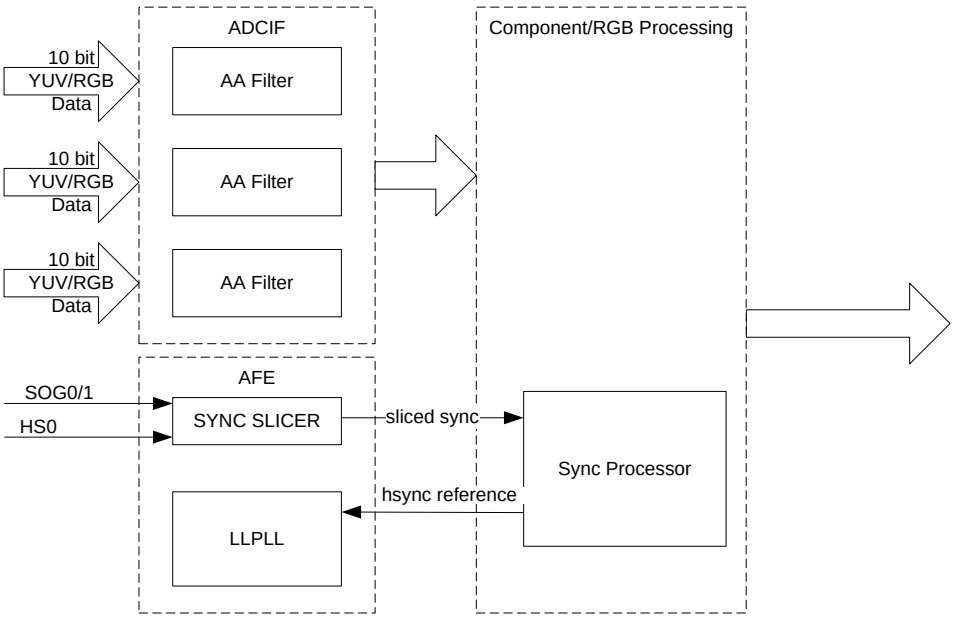


Figure 3.5. Component/RGB Processing Diagram

The SiI8784 device supports 480i/576i, 480p/576p, 720p, 1080i, and 1080p for standard and high definition resolutions. The SiI8784 device supports PC resolutions up to 1600 x 1200 @ 60 Hz (UXGA).

3.2.1.6. SCART Fast Blanking

VDC is designed to support SCART interface: Composite, RGB, and Fast Blanking.

The 4 channel 10-bit ADCs in AFE are mapped to CVBS, RED, GRN, and BLU inputs of SCART interface. A color space converter converts the digitized RGB data from RGB to YUV (BT601). Then the YUV data are resampled from 108 MHz to the 8Fsc frequency used in the 2D comb filter, and meanwhile the YUV444 data are converted to YUV422. These YUV422 data matched the timing of the 2D comb filter output 8Fsc Y/C data, and the two data streams are blended together according to the FB signal information, which indicates the current display source is from original RGB or Composite inputs.

The SCART_ASPECT information is from ASPECT0/1 comparator outputs of AFE, and their results are read-only status registers which can be handled by software.

3.2.2. Sync Processor

The Sync Processor block contains sophisticated digital circuitry that analyzes and extracts synchronization pulses from the incoming video stream. It generates filtered vertical and horizontal sync pulses. The Sync Processor includes Sync separation, format detection, and Sync stabilization.

- Sync Separation

The Sync Separation separates the HSync and VSync from the composite sync sliced from video decoder or SOG slicer.

- Sync Stabilization

Sync Stabilization does de-glitch, removes serration, and equalizes pulses from the sync signal. It also detects Macrovision protection status.

- Format Detection

The format detection detects vertical period and horizontal period and total line number per field.

3.2.3. VBI Decoder

The VBI Processing block slices and processes digitized VBI data from the video. Following are some of the features of the VBI block:

- 108 MHz operating with programmable down sampling
- Supports PAL standards
- Supports NTSC standards
- Enhanced Teletext parity and hamming 8/4 correction

Table 3.3 shows the supported VBI standards.

Table 3.3. Supported Standards

VBI Standard	Video Standard	Data Rate	Scan Lines	Data per Line	Encoding	Description
WSS 625	PAL SECAM	5 MHz	23 336	14 Bits	Phase Encoding. Each bit is transmitted using 6 bits of encoded data.	Wide Screen Signaling. Used for aspect ratio settings.
VPS	PAL SECAM	5 MHz	16	13 Bytes	Biphase Encoding. Each bit is effectively represented by 2 bits.	Video Programming System. Used in Germany for program/broadcast info.
CC	NTSC	0.5030 MHz	21	2 Bytes	Parity.	Closed Captioning for the hearing impaired.
XDS VChip	NTSC	0.5035 MHz	284	2 Bytes	Parity.	Extended Data Service. Used for MISC. NTSC services.
WSS 525 ID-1 CGMS	NTSC	0.4474 MHz	20	14 Bits	CRC.	Copy Guard Management System. Used for copy protection and aspect ratio.
Teletext	PAL SECAM	6.9375 MHz	6-22 318-334	42 Bytes	Encoded using parity, hamming 8/4 and hamming 24/18.	Teletext. Used for data transmissions in Europe.

3.3. Video Processing

The video processing block performs some necessary processing functions to the decoded video streams before they are outputted. There are also some measurement blocks inside to implement automatic Phase/Position/Gain adjustment functions.

3.3.1. Time Base Corrector

The Time Base Corrector (TBC) is designed to provide stable clock and video data for HDMI/MHL output. It uses a line buffer based architecture in lieu of a frame buffer to save cost and power. To keep HDMI/MHL output TMDS clock jitter in a safe range, the TBC output field frequency is limited to 50 Hz ±0.5% or 59.94 Hz/60 Hz ±0.5% as default. If the field frequency of input video is beyond this range, the display will be scrolling.

Composite video formats are supported by the TBC. 480i/576i component formats can be supported by the TBC if needed.

3.3.2. VBI Post Processor

The VBI Post Processor is used to transmit VBI data to DTV over the HDMI/MHL connection.

In case the raw VBI data i.e. digitized luma portion of the incoming video signal, or Teletext need to be transmitted to DTV over HDMI/MHL, they are embedded into the video stream and transmitted. As the decoded VBI data, they can be transmitted over HDMI or MHL using Vendor Specific Info Frame (VSIF).

3.3.3. De-interlacer and Edge Smoother

De-interlacing is designed to convert an interlaced (480i/576i) video signal to a progressive (480p/576p) video signal. BOB de-interlacing method is adopted to reduce cost and power consumption. An edge smoother is included to reduce the saw tooth artifacts generated by de-interlacing and to improve the picture quality.

The de-interlacer and edge smoother must be used together with the TBC.

3.3.4. Color Processing

Color Processing (CP) enables brightness, contrast, saturation, and hue controls for end users. It supports YCbCr color space only.

3.3.5. Auto Phase Detection

The Auto Phase Detection (APD) is a module used to search for the phases that can generate the best display quality. The desired phases, in general, can generate sharp and stable images, if the input image meets certain criteria during phase detection period. APD is an automatic algorithm that can be enabled or disabled by software. It can be applied to both VGA and Component inputs.

3.3.6. Auto Position Calibration

The Auto Position Calibration (APC) detects the active picture area of input video signal and adjusts the output timing so that the final picture can fit to the display properly.

3.3.7. Auto Gain Calibration

Slight mismatch of analog input channels including offset and gain may impact the picture quality. The SiI8784 device has been designed to keep the mismatches in an acceptable range (<0.5 dB). It is still important to calibrate these mismatches in some cases to achieve the most accurate picture. To help manufacturers finish this process efficiently, an Auto Gain Calibration (AGCWIN) mechanism is designed in the SiI8784 device. This mechanism automatically measures the digitalized signal levels through the AGCWIN module, calculates the correct values, and stores them into the external SPI Flash memory. These values can be used by firmware in user mode to compensate the analog mismatches.

3.4. Dual-mode HDMI/MHL Transmitter

The SiI8784 device incorporates the latest HDMI 1.4 and MHL 2 dual-mode transmitter. It multiplexes video and audio data into the HDMI/MHL stream and performs TMDS encoding. It contains digital video data capture and its processing block, digital audio data capture and its processing block, HDMI/MHL transmitter, and PHY. Figure 3.6 shows the dual-mode HDMI/MHL transmitter diagram.

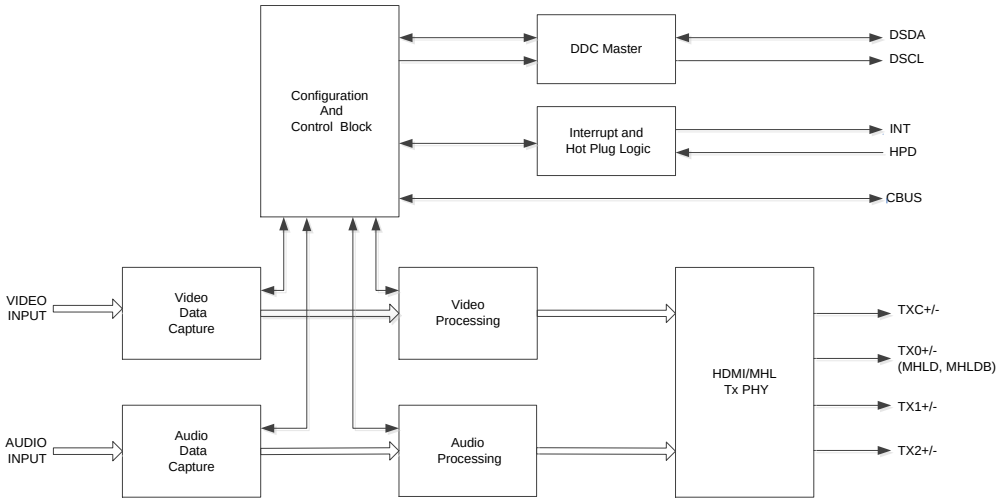


Figure 3.6. Dual-mode HDMI/MHL Transmitter Diagram

3.4.1. Video Data Capture Logic

The Video Data Capture Logic receives uncompressed digital video with a data width of 8 to 24 bits from the digital parallel video interface. The bus configurations support most standard video input formats as well as other widely used non-standard formats.

3.4.2. Video Processing Path

Figure 3.7 shows the video data processing stages. Each of the processing blocks can be bypassed by setting the appropriate register bits.

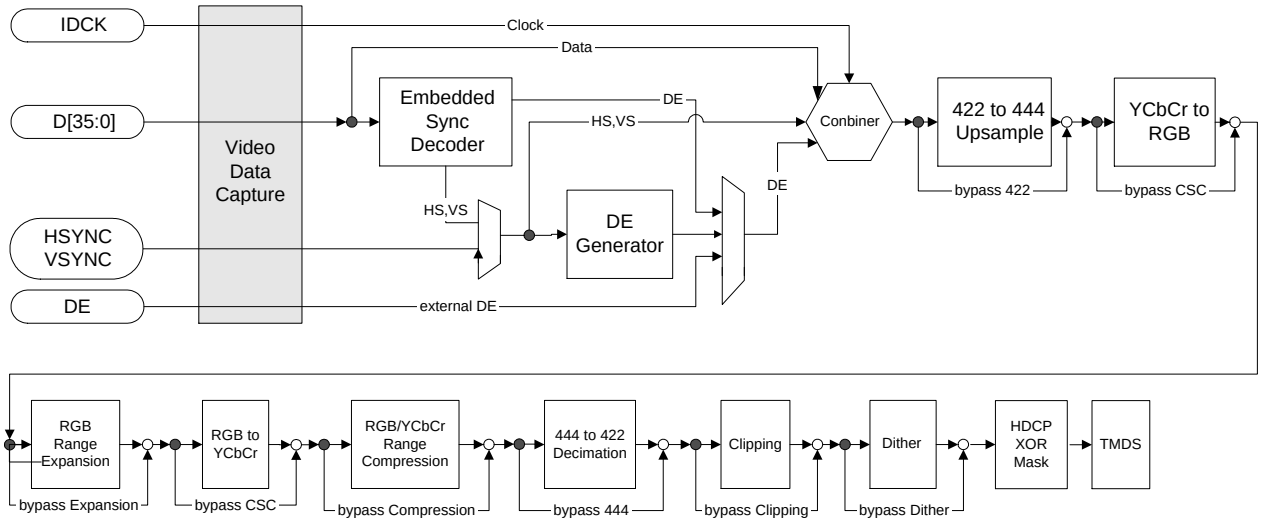


Figure 3.7. Transmitter Video Data Processing Path Embedded Sync Decoder

The input processor can create DE, HSYNC, and VSYNC signals using the start of active video (SAV) and end of active video (EAV) codes within the ITU-R BT.656-format video stream.

3.4.2.1. Data Enable Generator

The transmitter includes logic to construct a DE signal from the incoming HSYNC, VSYNC, and clock. Registers are programmed to enable the DE signal to define the size of the active display region.

3.4.2.2. Combiner

The clock, data, and sync information is combined into a complete set of signals required for TMDS encoding. From here, the signals are manipulated by the register-selected video processing blocks.

3.4.2.3. 422 to 444 Up-sampler

Chrominance up-sampling and down-sampling increase or decrease the number of chrominance samples in each line of video. Up-sampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

3.4.2.4. 444 to 422 Decimation

Decimation reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

3.4.2.5. Color Space Converters (CSC)

Two color space converters (CSCs) (YCbCr to RGB and RGB to YCbCr) are available to interface to the many video formats supplied by A/V processors and to provide full DVI backward compatibility. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

RGB to YCbCr

The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr formats. The HDMI AVI packet defines the color space of the incoming video.

Table 3.4. Color Space Versus Video Format

Video Format	Conversion	Formulas
		CE Mode 16-235 RGB
640 x 480	ITU-R BT.601	Y = 0.299R′ + 0.587G′ + 0.114B′ Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
480i	ITU-R BT.601	
576i	ITU-R BT.601	
480p	ITU-R BT.601	
576p	ITU-R BT.601	
240p	ITU-R BT.601	
288p	ITU-R BT.601	
720p	ITU-R BT.709	Y = 0.213R′ + 0.715G′ + 0.072B′ Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
1080i	ITU-R BT.709	
1080p	ITU-R BT.709	

YCbCr to RGB

The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. Refer to Table 3.5 for the detailed formulas. Note the difference between RGB range for CE modes and PC modes.

Table 3.5. YCbCr-to-RGB Color Space Conversion Formula

Format Change	Conversion	YCbCr Input Color Range [2, 3]
YCbCr 16-235 Input[2, 3] to RGB 16-235 Output[2, 3]	601[1]	R′ = Y + 1.371(Cr – 128) G′ = Y – 0.698(Cr – 128) – 0.336(Cb – 128) B′ = Y + 1.732(Cb – 128)
	709[1]	R′ = Y + 1.540(Cr – 128) G′ = Y – 0.459(Cr – 128) – 0.183(Cb – 128) B′ = Y + 1.816(Cb – 128)
YCbCr 16-235 Input[2, 3] to RGB 0-255 Output[2, 3]	601	R′ = 1.164((Y-16) + 1.371(Cr – 128)) G′ = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B′ = 1.164((Y-16) + 1.732(Cb – 128))
	709	R′ = 1.164((Y-16) + 1.540(Cr – 128)) G′ = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B′ = 1.164((Y-16) + 1.816(Cb – 128))

Notes:
1. No clipping can be done.
2. For 10-bit deep color, all occurrences of the values 16, 128, 235, and 255 should be multiplied by 4.
3. For 12-bit deep color, all occurrences of the values 16, 128, 235, and 255 should be multiplied by 16.

3.4.2.6. RGB Range Expansion

The SiI8784 input processor can scale the input color from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16 – 235 limited-range data into 0 – 255 for each video channel. When the range expansion and the YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16 – 240.

3.4.2.7. RGB/YCbCr Range Compression

When enabled by itself, the Range Compression Block compresses 0 – 255 full-range data into 16 – 235 limited-range data for each video channel. When enabled with the RGB to YCbCr converter, this block compresses to 16 – 240 for the Cb and Cr channels. The color range scaling is linear.

3.4.2.8. Clipping

The clipping block, when enabled, clips the values of the output video to 16 – 235 for RGB video or the Y channel, and to 16 – 240 for the Cb and Cr channels.

3.4.2.9. Dither

The dither block dithers internally processed data to 8, 10, or 12 bits for output on the HDMI link.

3.4.2.10. HDCP Encryption Engine/XOR Mask

The HDCP encryption engine contains the logic necessary to encrypt the incoming audio and video data and includes support for HDCP authentication and repeater checks. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes. An algorithm uses HDCP keys and a Key Selector Value (KSV) stored in the on-board ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle.

3.4.2.11. TMDS Digital Core

The TMDS digital core performs 8-to-10-bit TMDS encoding on the data received from the HDCP XOR mask. This data is sent to three TMDS differential data lines, along with a TMDS differential clock line. A resistor tied to the EXT_SWING pin controls the TMDS swing amplitude.

3.4.3. Audio Data Capture and Processing Logic

The SiI8784 device accepts digital audio over an S/PDIF interface, four I^2S inputs, or eight one-bit audio inputs.

3.4.3.1. S/PDIF

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets described in the HDMI Specification. The S/PDIF input supports audio sampling (Fs) rates from 32 to 192 kHz. A separate master clock input (MCLK), coherent with the S/PDIF input, is required for time-stamping purposes. *Coherent* means that the MCLK and S/PDIF have been created from the same clock source. This step usually uses the original MCLK to strobe out the S/PDIF from the sourcing chip. There is no setup or hold timing requirement on an input with respect to MCLK.

3.4.3.2. I^2S

Four I^2S inputs allow transmission of DVD-Audio or decoded Dolby Digital to A/V receivers and high-end displays. The interface works in slave mode, supports sample rate up to 192 kHz.

Register control allows the audio data to be down-sampled by one-half or one-fourth, so that the transmitter can be compatible with the attached display that supports lower sample rate audio only. Conversions from 192 to 48 kHz, from 176.4 to 44.1 kHz, from 96 to 48 kHz, and from 88.2 to 44.1 kHz are supported. Audio data can only be down-sampled on 2-channel audio.

The appropriate registers must be configured to describe the audio format provided to the SiI8784 input processor. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets.

Table 3.6 shows the MCLK frequencies that support seven audio sample rates.

Table 3.6. Supported MCLK Frequencies

Multiple of Fs	I^2S and S/PDIF Supported MCLK Rates						
	Audio Sample Rate, Fs						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	67.737 MHz	73.728 MHz
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz	—	—
768	24.576 MHz	33.869 MHz	36.864 MHz	67.738 MHz	73.728 MHz	—	—
1024	32.768 MHz	45.158 MHz	49.152 MHz	—	—	—	—
1152	36.864 MHz	50.803 MHz	55.296 MHz	—	—	—	—

3.5. Control Logic

3.5.1. Internal Microcontroller

As shown in Figure 3.1 on page 7, an 8-bit 8051 compatible microcontroller is integrated in the SiI8784 device. It contains 3 KB data RAM and 96 KB code RAM. The code can be loaded into code RAM from external SPI Flash or EEPROM memory automatically after power on. If the check sum of the code data is correct, the code will be executed. Otherwise the internal microcontroller is disabled and the chip can be controlled by external controller through I^2C bus. The internal controller can access all the internal registers directly over the internal bus. The 8051 microcontroller runs at the crystal clock of 24 MHz.

When the booting procedure is finished, the SPI interface will be handed over to the 8051 SPI module so that firmware can read/write the external memory if needed.

The internal controller can also operate other peripherals through the I^2C bus of the SiI8784 device by setting it to the master mode.

3.5.1.1. Data Structure of External SPI Memory

Figure 3.8 shows the memory structure which is required for the internal microcontroller to load the code correctly.

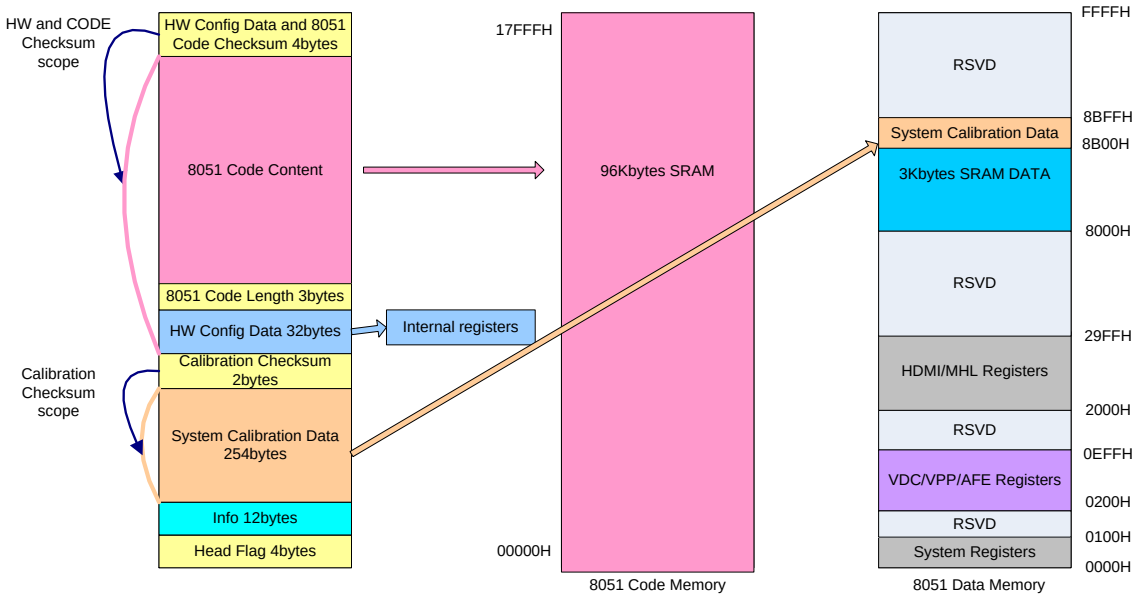


Figure 3.8. External Memory Structure

Table 3.7. Head Flags

EEPROM/Flash Address	EEPROM/Flash Content
00000H	Head0 'S'
00001H	Head1 'I'
00002H	Head2 'M'
00003H	Head3 'G'

Note: The head flag will be four bytes ASCII code of 'S', 'I', 'M', 'G'.

Table 3.8. Info Bytes

EEPROM/Flash Address	EEPROM/Flash Content
00004H	SPI PARAMETER.
00005H	Calibration Version (low byte)
00006H	Calibration Version.
00007H	Calibration Version (high byte).
00008H	Code Version (low byte).
00009H	Code Version.
0000AH	Code Version (high byte).
0000BH	Reserved.
0000CH	Reserved.
0000DH	Reserved.
0000EH	Reserved.
0000FH	Reserved.

Note: The info bytes contain the information about the feature of Max read frequency of external EEPROM/Flash, the calibration version, and the code version. It occupies 12 bytes.

Table 3.9. SPI Parameter

SPI Parameter	Description
0x00	2 MHz baud rate to access SPI Flash/EEPROM.
0x01	24 MHz baud rate to access SPI Flash/EEPROM.

Table 3.10. Calibration Checksum

EEPROM/Flash Address	EEPROM/Flash Content
0010EH	Calibration Checksum (low byte).
0010FH	Calibration Checksum (high byte).

Note: The calibration checksum is two bytes which locates at the last site of 256 size calibration data.

Table 3.11. HW Configuration Data

EEPROM/Flash Address	EEPROM/Flash Content
00110H	BT_SPI_PINMUX_SEL. 00H – SPI function 01H – Reserved. Don't use 02H – Reserved. Don't use
00111H..0012FH	Reserved.

Table 3.12. 8051 Code Size

EEPROM/Flash Address	EEPROM/Flash Content
00130H	Code Size (low byte).
00131H	Code Size.
00132H	Code Size (high byte).

Table 3.13. HW Configuration Data and Code Checksum

EEPROM/Flash Address	EEPROM/Flash Content
00133H + code size	Code Checksum0 (lowest byte).
00134H + code size	Code Checksum1.
00135H + code size	Code Checksum2.
00136H + code size	Code Checksum3 (highest byte).

The boot module tries to load data from external device and write into chip SRAM. The 8051 code content is written into the 96K bytes SRAM of 8051. The 256 system calibration is written into the high 3 K bytes SRAM in data memory.

For details on the selection of the SPI Flash memory, refer to the relevant Application Note (SiI-AN-1108).

3.5.2. Registers

The register block incorporates all the registers required for configuring and managing the SiI8784 device. These registers are used to perform AFE processing, VDC processing, MHL/HDMI processing, and all other control functions.

3.5.3. I²C Bus

The local I²C slave bus provides the host with communication to the entire system. The controller I²C interface on the SiI8784 device (signals CSCL and CSDA) is a slave interface, which is capable of running up to 400 kHz.

All functions of the SiI8784 device are controlled and observed with I²C registers. Device addresses can be altered with the level of the CI2CA signal. Table 3.14 shows the device addresses as altered by the level of the CI2CA signal.

Table 3.14. Control of Transmitter I²C Address with CI2CA Signal

CI2CA = 0	CI2CA = 1	Purpose
0x8C	0x8E	System Control and Status
0x84	0x84	VD_DPGA VD_SIGNALROUTING
0x86	0x86	VD_VBI
0x8A	0x8A	VD_VDREG VD_ADCIF
0x92	0x92	VD_SYNCPROC
0x96	0x96	VD_ADCSTATUS VD_VPP Edge Smooth INT
0xDA	0xDA	FPGA APD ADC_WIN
0x9C	0x9C	VidPath Calibration
0xD8	0xD8	AFE
0x72	0x76	HW_TPI TX Page 0/2
0x7A	0x7E	TX Page 1
0x90	0x94	Reserved
0xC0	0xC4	CEC 1.6
0x60	0x60	TX PHY
0xC8	0xCC	CBUS

Note: When the internal microcontroller is enabled, the I²C bus is taken over by the firmware. It can work as both master and slave mode, and the addresses are alterable.

3.5.4. Interrupt

The SiI8784 device contains a configurable interrupt generator with an open-drain type output pin. It can be used to notify application processor (if there is application processor) to handle some events.

3.5.5. GPIOs

There are five general purpose IO pins on the SiI8784 device. Generally they can be used to detect the cable plug-in status, but they can be used for other purposes as well.

Table 3.15. List of GPIOs

Name	Type	Pull up/down[2]	Reset Status
GPIO0[1]	IO	Pull down	I
GPIO1	IO	Pull up	I
GPIO2	IO	Pull up	I
GPIO3	IO	Pull up	I
GPIO4	IO	Pull up	I

Notes:

1. GPIO0 is also used as CI2CA pin to decide the I^2C slave address during reset.
2. The internal Pull up/down resistors are fixed and weak just to avoid floating input level when they are left unconnected. Peripheral circuits should not rely on them. 10 K or smaller resistors are recommended for external pull up/down circuit to override them if needed.

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Notes
VP2V5A	Analog Power for ADC	–0.3	—	3.0	V	1, 2
VP2V5D	Digital Power for ADC	–0.3	—	3.0	V	1, 2
VP2V5_SLICER	Analog Power for SOG Slicer	–0.3	—	3.0	V	1, 2
VP1V0_PLL	Power for APLL and LLPLL	–0.3	—	1.2	V	1, 2
VCC10_TPLL	TCI PLL Power	–0.3	—	1.2	V	1, 2
AVCC_PLL	Analog PLL Power of HDMI/MHLTX	–0.3	—	1.2	V	1, 2
AVCC	Power for HDMI/MHL TX	–0.3	—	1.2	V	1, 2
AVCC3V3_CBUS	Power for CBUS I/O	–0.3	—	4.0	V	1, 2
CVCC10	Power for Digital Core	–0.3	—	1.2	V	1, 2
VDDIO3V3	Power for Digital I/O	–0.3	—	4.0	V	1, 2
XTALVCC33	Power for XTAL	–0.3	—	4.0	V	1, 2
V_I	Digital Input Voltage	–0.3	—	VDDIO + 0.3	V	1, 2
V_O	Digital Output Voltage	–0.3	—	VDDIO + 0.3	V	1, 2
AV_I	Analog Input Voltage	-0.3	—	VP2V5A + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V Tolerant Pins	–0.3	—	5.5	V	—
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under normal operating conditions.

4.2. Normal Operating Conditions

Table 4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VP2V5A	Analog Power for ADC	2.375	2.50	2.625	V	2
I_{VP2V5A}	Total Current Consumption of VP2V5A	—	350	—	mA	4, 8
		—	90	—	mA	5, 8
		—	260	—	mA	6, 8
		—	260	—	mA	7, 8
VP2V5D	Digital Power for ADC	2.375	2.50	2.625	V	—
I_{VP2V5D}	Total Current Consumption of VP2V5D	—	9	—	mA	4, 8
		—	2.5	—	mA	5, 8
		—	9	—	mA	6, 8
		—	10	—	mA	7, 8
VP2V5_SLICER	Analog Power for SOG Slicer	2.375	2.50	2.625	V	2
I_{VP2V5_SLICER}	Current Consumption of VP2V5_SLICER	—	3	—	mA	6, 8
VP1V0_PLL	Power for APLL and LLPLL	0.95	1.00	1.05	V	3
I_{VP1V0_PLL}	Current Consumption of VP1V0_PLL	—	20	—	mA	7, 8
VCC10_TPLL	TCI PLL Power	0.95	1.00	1.05	V	3
I_{VCC10_TPLL}	Current Consumption of VCC10_TPLL	—	3.5	—	mA	5, 8
AVCC_PLL	Analog PLL Power of HDMI/MHLTX	0.95	1.00	1.05	V	3
I_{AVCC_PLL}	Current Consumption of AVCC_PLL	—	4.5	—	mA	7, 8
		—	8.5	—	mA	6, 9
AVCC	Power for HDMI/MHL TX	0.95	1.00	1.05	V	—
I_{AVCC}	Current Consumption of AVCC	—	4.5	—	mA	7, 8
		—	10	—	mA	6, 9
CVCC10	Power for Digital Core	0.95	1.00	1.05	V	—
I_{CVCC10}	Total Current Consumption of CVCC10	—	70	—	mA	4, 8
		—	65	—	mA	5, 8
		—	80	—	mA	6, 8
		—	85	—	mA	7, 8
		—	85	—	mA	4, 9
		—	70	—	mA	5, 9
		—	100	—	mA	6, 9
VDDIO3V3	Power for Digital I/O	3.135	3.30	3.465	V	—
$I_{VDDIO3V3}$	Current Consumption of VDDIO3V3	—	2	—	mA	4, 8
		—	2	—	mA	5, 8
		—	7	—	mA	6, 8
		—	8	—	mA	7, 8
		—	40	—	mA	4, 9
		—	55	—	mA	5, 9
		—	60	—	mA	6, 9
AVCC3V3_CBUS	Power for CBUS I/O	3.135	3.30	3.465	V	—
$I_{AVCC3V3\_CBUS}$	Current Consumption of AVCC3V3_CBUS	—	8	—	mA	6, 9
XTALVCC33	Power for XTAL	3.135	3.30	3.465	V	—
$I_{XTALVCC33}$	Current Consumption of XTALVCC33	—	3.5	—	mA	6, 8
TA	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	25.6	°C/W	1

Table 4.2. Normal Operating Conditions (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Notes
Θ_{jc}	Case Thermal Resistance (Theta JC)	—	—	11.9	—	—

Notes:
1. Airflow at 0 m/s. Package ePad soldered to PCB.
2. The power ripple must be below 60 mVpp to avoid video quality detrition.
3. Avoid any noise coupling to PLL power rails.
4. Measured with SCART input.
5. Measured with CVBS input.
6. Measured with YPbPr 1080p60 input.
7. Measured with UXGA60 input.
8. HDMI output mode.
9. MHL output mode.

4.3. ESD Specifications

Table 4.3. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
Latch up	ESD Latch up	± 200	—	—	mA	1, 2
HBM	Human Body Model	2000	—	—	V	3
MM	Machine Model	200	—	—	V	4
CDM	Charged Device Model	500	—	—	V	5

Notes:
1. At 70 °C.
2. Measured as per JESD78B standard.
3. Measured as per JESD22-A114 standard.
4. Measured as per JESD22-A115 standard.
5. Measured as per JESD22-C101 standard.

4.4. DC Specifications

Table 4.4. Digital I/O Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
Digital Inputs							
V_{IL}	Input Low Voltage	—	—	—	0.8	V	1
V_{IH}	Input High Voltage	—	2.0	—	—	V	1
V_{TH+}	Schmitt Trigger LOW to HIGH Threshold	—	1.61	1.69	1.77	V	1
V_{TH-}	Schmitt Trigger HIGH to LOW threshold	—	1.18	1.27	1.35	V	1
IIL	Input Leakage Current	—	–10	—	10	µA	1
RPU	Pull-up Resistor	—	27	38	59	KΩ	1
RPD	Pull-down Resistor	—	31	46	80	KΩ	1
V_{TH+DDC}	Schmitt Trigger LOW to HIGH Threshold of DSCL and DSDA Pins	—	3	—	—	V	—
V_{TH-DDC}	Schmitt Trigger HIGH to LOW Threshold of DSCL and DSDA Pins	—	—	—	1.5	V	—
V_{TH+CEC}	Schmitt Trigger LOW to HIGH Threshold of CEC Pin	—	2	—	—	V	—
V_{TH-CEC}	Schmitt Trigger HIGH to LOW Threshold of CEC Pin	—	—	—	0.8	V	—
RPU_{CEC}	Pull-up Resistor on CEC Pin	—	24.3	27	29.7	KΩ	—
V_{TH+I2C}	Schmitt Trigger LOW to HIGH Threshold of LSCL and LSDA Pins	—	2.0	—	—	V	2
		—	3.0	—	—	V	3
V_{TH-I2C}	Schmitt Trigger HIGH to LOW Threshold of LSCL and LSDA Pins	—	—	—	0.8	V	2
		—	—	—	1.5	V	3
Digital Outputs							
V_{OH}	HIGH-level Output Voltage	I_{OH} = 8mA	2.4	—	—	V	1
V_{OL}	LOW-level Output Voltage	I_{OL} = –8mA	—	—	0.4	V	1
I_{OZ}	Tri-state Output Leakage Current	—	–10	—	10	µA	1
V_{OH_CEC}	HIGH-level Output Voltage of CEC Pin	I_{OH} = 100µA	2.5	—	—	V	—
V_{OL_CEC}	LOW-level Output Voltage of CEC Pin	I_{OL} = –100µA	—	—	0.4	V	—

Notes:
1. Applies to general digital IOs.
2. Compatible to 3.3 V I²C level in default.
3. Compatible to 5 V DDC level (need to be configured by register).

Table 4.5. HDMI TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SWING}	Single-ended Output Swing Voltage	R_{LOAD} = 50 Ω	400	—	600	mV
V_H	Single-ended High-level Output Voltage	—	AV_{CC} – 200	—	AV_{CC} + 10	mV
V_L	Single-ended Low-level Output Voltage	—	AV_{CC} – 700	—	AV_{CC} – 400	mV
I_{DOS}	Differential output short-circuit current	VOUT = 0 V	—	—	5	µA

Table 4.6. MHL TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SE_HIGH}	Single-ended HIGH-level Output voltage	—	V_{TERM} - 540	—	V_{TERM} + 10	mV
V_{SE_LOW}	Single-ended LOW-level Output voltage	—	V_{TERM} - 1760	—	V_{TERM} - 700	mV
V_{OFF}*	Single-ended Standby (off) Output Voltage	—	V_{TERM} -10	—	V_{TERM} + 10	mV
$V_{DFSWING}$	Differential Output Swing Amplitude	RLOAD = 50 Ω	600	—	1000	mV
$V_{CMSWING}$	Common Mode Output Swing	RLOAD = 50 Ω single-ended	360	—	Min (720, 0.85×VDFSWING)	mV

*** Note:**

V_{OFF} is the source output voltage when terminated to V_{TERM} through R_{T1}, and the source device is in standby mode or power off mode.

Table 4.7. CBUS DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TERM_CBUS}	CBUS Termination Voltage	—	1.7	—	1.9	V
V_{IH_CBUS}	HIGH-level Input Voltage	—	1.0	—	—	V
V_{IL_CBUS}	LOW-level Input Voltage	—	—	—	0.6	V
V_{OH_CBUS}	HIGH-level Output Voltage	IOVCC18 = 1.8 V, 85 °C	1.5	—	—	V
V_{OL_CBUS}	LOW-level Output Voltage	IOVCC18 = 1.8 V, 85 °C	—	—	0.2	V
I_{OH_CBUS}	HIGH-output Drive Current	V_{OH} = 1.5 V	2	—	—	mA
I_{OL_CBUS}	LOW-output Drive Current	V_{OL} = 0.2 V	300	—	—	µA
I_{IL}/I_{IH}	Input Leakage Current	High-impedance	–1.0	—	1.0	µA
$Z_{CBUS\_SRC\_DISCOVER}$	Pull-up Resistance – Discovery	—	9	10	11	kΩ
$Z_{CBUS\_SRC\_ON}$	Pull-up Resistance – ON	—	4	5	6	kΩ
$Z_{RID\_MHL\_ACCEPT}$	R_ID range identified as MHL	—	800	1000	1200	Ω
$Z_{RID\_MHL\_REJECT}$	R_ID identified as not MHL	—	<500	—	>1600	Ω

4.5. AC Specifications

Table 4.8. Analog Front-end Electrical Specifications

Analog Input						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
—	Input Capacitance	—	—	5	—	pF
V_{FSR}	Analog Input Range	—	0.3	—	1.2	V
—	Clamp Level	—	0.25	—	0.85	V
V_{OAR}	Offset Adjustment Range	—	–0.5	—	+ 0.5	V
—	Offset Adjustment Resolution	—	—	10	—	Bits
BW	Input Analog Filter Bandwidth	—	50	—	600	MHz
—	Gain Adjustment Range	—	–6	—	+ 6	dB
A/D Converters						
—	Conversion Rate	—	25	—	170	MHz
N	ADC Resolution	—	—	10	—	Bits
INL	Integral Nonlinearity	580 mVpp, 2.8 kHz Ramp Wave Sampling Rate: 55 MHz PGA Gain: 0 dB LPF Bandwidth: 50 MHz	—	4	—	LSB
DNL	Differential Nonlinearity		—	1	—	LSB
NMC	No Missing Codes	—	Guaranteed			—
ENOB	Effective Number Of Bits	300 mVpp, 1.1 MHz Sine Wave Sampling Rate: 165 MHz PGA Gain: 0 dB LPF Bandwidth: 400 MHz	—	7.5	—	Bits
PLL						
—	Clock Frequency Range	—	25	—	170	MHz
—	Period Jitter	—	—	—	450	ps
—	Phase Adjustment	—	—	11.25	—	Degree/Step
—	Duty Cycle	—	45	50	55	%
Video Buffer						
DP	Differential Phase	—	—	—	4	Degrees
DG	Differential Gain	—	—	—	4	%
THD	Total Harmonic Distortion	700 mVpp, 4 MHz Sine Wave Load = 37.5 Ω Internal Clamp: OFF	—	–48	—	dB

Table 4.9. HDMI/MHL Output AC Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MHL Mode						
FMHL	Link Clock Frequency	—	25	—	75	MHz
FPIXEL	Pixel Clock Frequency	—	25	—	75	MHz
TMHL	Link Clock Period	—	13.33	—	40	ns
TBIT	Bit Time on Link	—	0.444	—	1.33	ns
TR_DF	Differential Swing LOW-to-HIGH Transition Time	R_{LOAD} = 100 Ω Differential Mode	75	—	—	ps
TF_DF	Differential Swing HIGH-to-LOW Transition Time		75	—	—	ps
TR_CM	Common Mode Clock Swing LOW-to-HIGH Transition Time	R_{LOAD} = 30 Ω Common Mode	600	—	2500	ps
TF_CM	Common Mode Clock Swing HIGH-to-LOW Transition Time		600	—	2500	ps
TSKEW_DF	Differential Intrapair Skew	—	—	—	50	ps
TSKEW_CM	Common Mode Intrapair Skew	—	—	—	50	ps
%TMHL	Clock Duty Cycle	—	35	—	65	%
TMJIT	MHL Clock Jitter	—	—	—	$0.25T_{BIT}$+200	ps
HDMI Mode						
TTXDPS	Intrapair Differential Output Skew	—	—	0.03	0.15	TBIT
TTXRT	Data/Clock Rise Time	20% – 80%	75	—	—	ps
TTXFT	Data/Clock Fall Time	20% – 80%	75	—	—	ps
FTXC	Differential Output Clock Frequency	—	25	—	165	MHz
TTXC	Differential Output Clock Period	—	6.06	—	40	ns
TDUTY	Differential Output Clock Duty Cycle	—	40%	—	60%	TTXC
TOJIT	Differential Output Clock Jitter	—	—	—	0.25	TBIT

Table 4.10. CBUS Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{RISE}	Rise Time	CL = 560 pF	5	—	200	ns	—
T_{FALL}	Fall Time	CL = 560 pF	5	—	200	ns	—
ΔT_{RF}	Rise-to-Fall Time Difference	—	—	—	100	ns	—
T_{BIT}	Bit Time (1 MHz)	—	0.8	—	1.2	µsec	—
$T_{SRC:PULSE\_WIDTH}$	Discovery Pulse Width (High Time, Float Time)	—	80	100	120	µsec	—
$T_{SRC:CONN}$	CBUS HIGH detect to connected state	—	—	—	240	µsec	1
$T_{CBUS\_SRC\_ON}$	Connected State to ZCBUS_SRC_ON enabled	—	—	—	120	µsec	—
$T_{ARBITRATE}$	Connected state to First CBUS Packet allowed	—	500	—	—	µsec	2
$N_{SRC\_PULSE\_COUNT}$	Discovery Pulse Count attempted	—	6	—	20	pulses	3
$T_{BIT\_VARY\_PACKET}$	Bit Time variation within the packet	—	–1%	—	1%	T_{BIT}	4

Notes:

1. This parameter is the length of time from when the source detects a HIGH on CBUS (held HIGH by the sink at the end of a discovery drive-and-float pulse), to when the source switches CBUS impedance to ZCBUS_SRC_ON and CBUS becomes active. *Active* means ready to receive the first packet.
2. Source and sink must wait at least this long before beginning first arbitration on CBUS.
3. A sink that detects at least $N_{SINK\_PULSE\_COUNT}${min} changes its pull-down resistance on CBUS from $Z_{CBUS\_SINK\_DISCOVER}$ to $Z_{CBUS\_SINK\_ON}$.
4. Bits driven by the initiator within one packet should match the mean bit time in the packet by this limit.

Table 4.11. I²S Audio Input Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
FS_I2S	Sample Rate	—	32	—	192	kHz	—
TSCKCYC	I²S Cycle Time	—	—	1.0	—	UI	Figure 5.4
TSCKDUTY	I²S Duty Cycle	—	90	—	110	%UI	Figure 5.4
TI2SSU	I²S Setup Time	—	15	—	—	ns	Figure 5.4
TI2SHD	I²S Hold Time	—	1	—	—	ns	Figure 5.4

Table 4.12. S/PDIF Input Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
FS_SPDIF	Sample Rate	—	32	—	192	kHz	—	—
TSPCYC	S/PDIF Cycle Time	—	—	—	2.0	UI	Figure 5.5	1
TSPDUTY	S/PDIF Duty Cycle	—	90	—	110	%UI	Figure 5.5	1
TAUDDLY	Audio Pipeline Delay	—	—	30	70	µs	—	2

Notes:
1. Proportional to unit time (UI), according to the sample rate. Refer to the I²S or S/PDIF Specifications.
2. Audio pipeline delay measured from transmitter input signals to TMDS output. The video path delay is insignificant.

4.6. Control Signal Timing Specifications

Table 4.13. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid Delay from SCL falling edge on READ command	CL = 400pF	—	—	700	ns	Figure 5.1	1, 2
T_{RESET}	RESET_N Signal LOW Time required for reset	—	5000	—	—	ns	Figure 5.2, Figure 5.3	3

Notes:
1. All standard-mode (100 kHz) I²C timing requirements are guaranteed by design. These timings apply to the slave I²C port (signals LSDA and LSCL).
2. Operation of I²C signals above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL} (see Table 4.4 on page 26). For these levels, I²C speeds up to 400 kHz are supported.
3. Reset on RESET_N signal can be LOW as CVCC10 and VDDIO33 become stable, or pulled LOW for at least T_{RESET}.

5. Timing Diagrams

5.1. I²C Bus Timing Diagrams

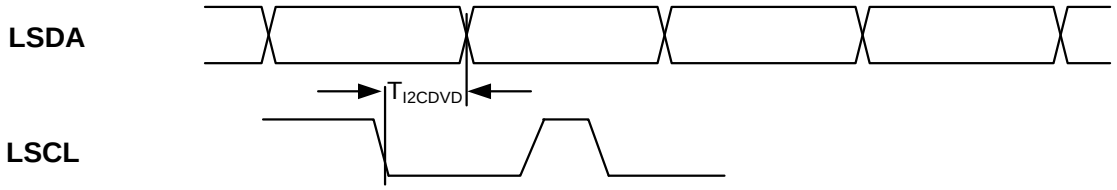


Figure 5.1. I²C Data Valid Delay (Driving Read Cycle Data)

5.2. Reset Timing Diagram

All power rails must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET_N is HIGH. RESET_N must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET_N LOW until T_{RESET} after stable power (Figure 5.2) or by pulling RESET_N LOW from a HIGH state (Figure 5.3) for at least T_{RESET}.

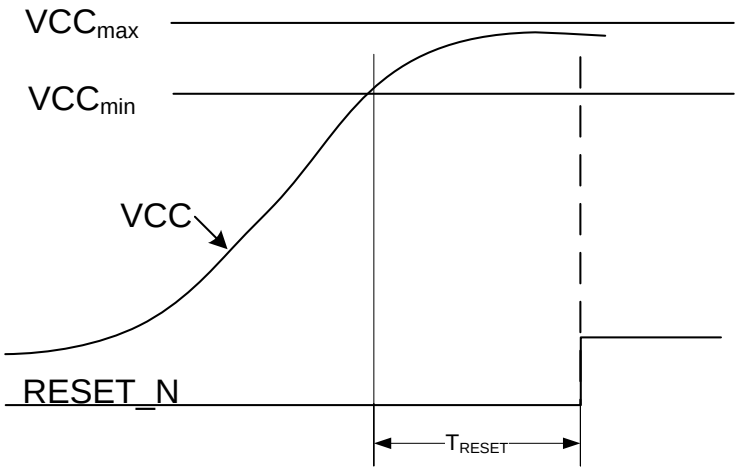


Figure 5.2. Conditions for Use of RESET_N

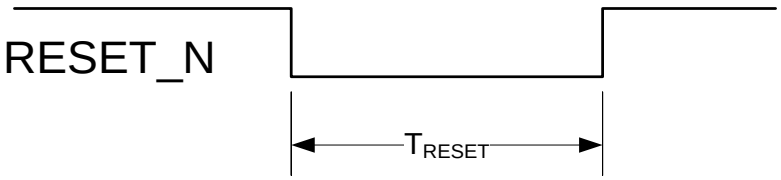


Figure 5.3. RESET_N Minimum Timings

5.3. Audio Timing Diagrams

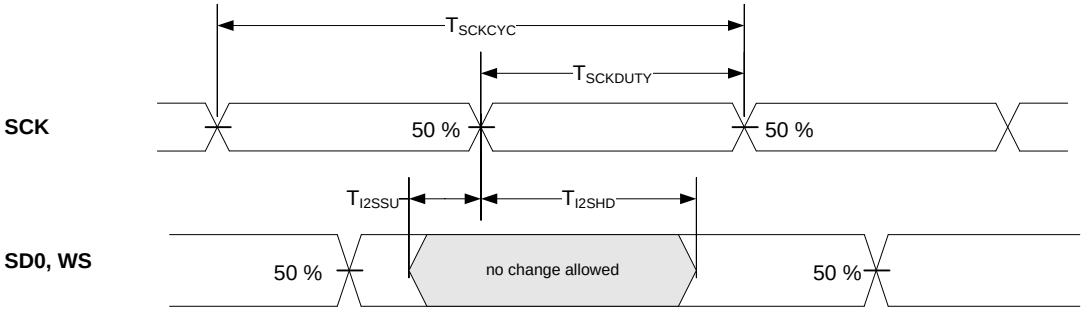


Figure 5.4. I²S Timings

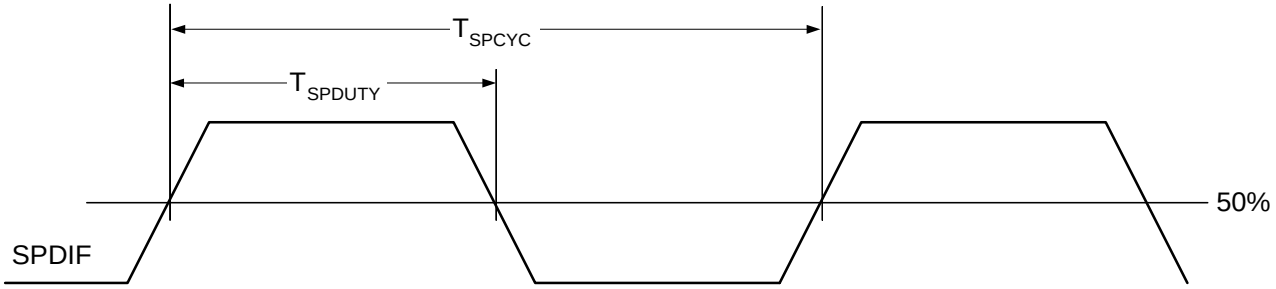


Figure 5.5. S/PDIF Timings

6. Pin Diagram and Description

6.1. Pin Diagram

Figure 6.1 shows the pin diagram of the SiI8784 device. Individual pin functions are described in the Pin Descriptions section on the next page. The package is an 88-pin 10 mm × 10 mm, 0.9 mm pitch QFN with ePad, which ***must*** be connected to ground.

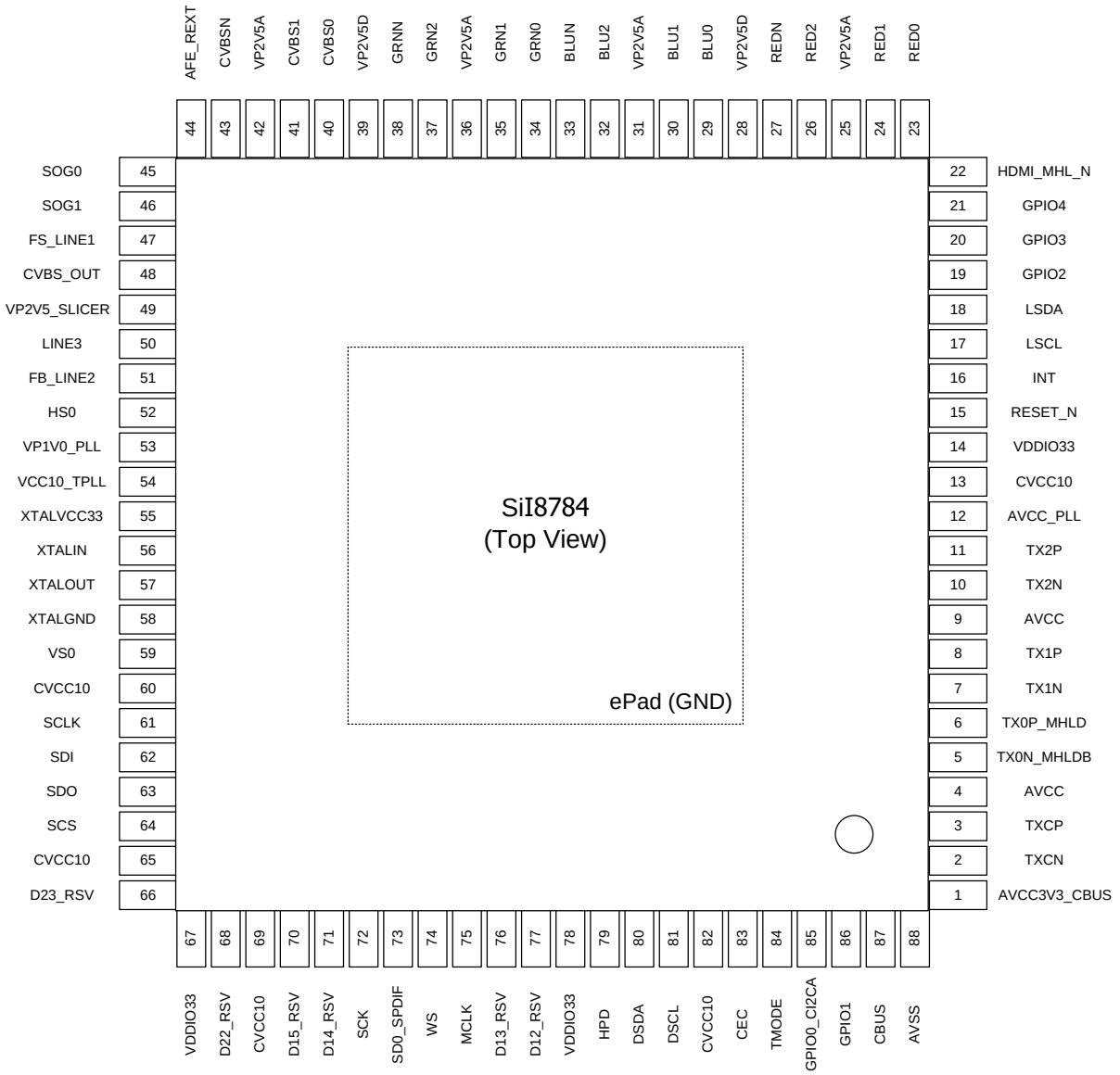


Figure 6.1. Pin Diagram

6.2. Pin Descriptions

The following tables provide the pin descriptions for the SiI8784 device.

6.2.1. AFE Pins

Table 6.1. AFE Input/Output Pins

Pin Name	Pin	Type	Direction	Description	Notes
RED0	23	Analog	Input	RED Input 0.	1
RED1	24	Analog	Input	RED Input 1.	1
RED2	26	Analog	Input	RED Input 2.	1
REDN	27	Analog	Input	RED Negative Input.	2
BLU0	29	Analog	Input	BLUE Input 0.	1
BLU1	30	Analog	Input	BLUE Input 1.	1
BLU2	32	Analog	Input	BLUE Input 2.	1
BLUN	33	Analog	Input	BLUE Negative Input.	2
GRN0	34	Analog	Input	GREEN Input 0.	1
GRN1	35	Analog	Input	GREEN Input 1.	1
GRN2	37	Analog	Input	GREEN Input 2.	1
GRNN	38	Analog	Input	GREEN Negative Input.	2
CVBS0	40	Analog	Input	CVBS Input 0.	1
CVBS1	41	Analog	Input	CVBS Input 1.	1
CVBSN	43	Analog	Input	CVBS Negative Input.	2
AFE_REXT	44	Analog	Passive	External Bias Resistor. Must connect a 12 K, 1% resistor to ground.	—
SOG0	45	Analog	Input	SOG Input 0.	—
SOG1	46	Analog	Input	SOG Input 1.	—
FS_LINE1	47	Analog	Input	FS (SCART) or LINE1 (D-Terminal) Input.	—
FB_LINE2	51	Analog	Input	FB (SCART) or LINE2 (D-Terminal) Input.	—
LINE3	50	Analog	Input	LINE3 (D-Terminal) Input.	—
HS0	52	Analog	Input	HSync Input.	—
VS0	59	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Input	VSync Input.	—
CVBS_OUT	48	Analog	Output	CVBS Output. Connect a 75 Ω resistor to ground when CVBS output is enabled.	—

Notes:

1. A 47nF couple capacitor is required when this pin is used.
2. Must connect a 0.1uF capacitor to ground when the corresponding input channel is used.

6.2.2. Audio Input Pins

Table 6.2. Audio Input Pins

Pin Name	Pin	Type	Direction	Description
SCK	72	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Input	I²S Bit Clock Input.
WS	74	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Input	I²S Word Select Signal Input.
SD0_SPDIF	73	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Input	I²S Data Input or SPDIF Input.
MCLK	75	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Input	Master Clock Input.

6.2.3. Configuration and Control Pins

Table 6.3. Configuration and Control Pins

Pin Name	Pin	Type	Direction	Description
INT	16	LVTTL Open Drain 5 V Tolerant	Output	Interrupt Pin.
RESET_N	15	LVTTL Schmitt Trigger 5 V Tolerant	Input	External Reset Signal. Active LOW.
LSCL	17	Open Drain Schmitt Trigger 5 V Tolerant	IO	Local I^2C Bus Clock. Compatible with 5V and 3.3V I^2C standard.
LSDA	18	Open Drain Schmitt Trigger 5 V Tolerant	IO	Local I^2C Bus Data. Compatible with 5V and 3.3V I^2C standard.
TMODE	84	Test Pin	Input	Reserved for test. This pin must be tied low during the normal operation.
GPIO0_CI2CA	85	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	IO	General GPIOs. It also is used to select local I^2C slave address during reset when the internal 8051 is not used.
GPIO1	86	LVTTL Schmitt Trigger 5 V Tolerant Pull-up	IO	General GPIOs.
GPIO2	19	LVTTL Schmitt Trigger 5 V Tolerant Pull-up	IO	General GPIOs.
GPIO3	20	LVTTL Schmitt Trigger 5 V Tolerant Pull-up	IO	General GPIOs.
GPIO4	21	LVTTL Schmitt Trigger 5 V Tolerant Pull-up	IO	General GPIOs.
HDMI_MHL_N	22	LVTTL Schmitt Trigger 5 V Tolerant Pull-up	Input	MHL and HDMI Select. High – HDMI Low – MHL

6.2.4. HDMI/MHL Data Pins

Table 6.4. HDMI/MHL Data Pins

Pin Name	Pin	Type	Direction	Description
TX0P_MHLD	6	TMDS	Output	TMDS Output Data Pairs for HDMI output. It is also used as MHL data pairs for MHL output.
TX0N_MHLDB	5	TMDS	Output	TMDS Output Data Pairs for HDMI output.
TX1P	8	TMDS	Output	TMDS Output Data Pairs for HDMI output.
TX1N	7	TMDS	Output	TMDS Output Data Pairs for HDMI output.
TX2P	11	TMDS	Output	TMDS Output Data Pairs for HDMI output.
TX2N	10	TMDS	Output	TMDS Output Data Pairs for HDMI output.
TXCP	3	TMDS	Output	TMDS Output Data Pairs for HDMI output.
TXCN	2	TMDS	Output	TMDS Output Data Pairs for HDMI output.
DSDA	80	Open Drain Schmitt Trigger 5 V Tolerant	IO	DDC Signals for HDMI output. Compatible with 5 V I^2C standard. Must connect pullup resistor to make sure DDC functions normal for both of HDMI and MHL output modes.
DSCL	81			
HPD	79	LVTTL Schmitt Trigger 5 V Tolerant	Input	Hot Plug Detect Input. It is recommended to connect a 47 K pulldown resistor to ground for HDMI output.
CEC	83	CEC Pull-up	IO	CEC Port.
CBUS	87	Analog 5 V Tolerant	IO	CBUS Port. It can be connected to HPD pin in the case of outputting MHL over HDMI Type-A connector.

6.2.5. SPI Interface Pins

Table 6.5. SPI Interface Pins

Pin Name	Pin	Type	Direction	Description
SCLK	61	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Output	SPI clock output. Keep HiZ when RESET_N is low.
SDI	62	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Input	SPI Data Input.
SDO	63	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Output	SPI Data Output. Keep HiZ when RESET_N is low.
SCS	64	LVTTL Schmitt Trigger 5 V Tolerant Pull-down	Output	SPI Chip Enable. Keep HiZ when RESET_N is low.

6.2.6. Power and Ground Connections

Table 6.6. Power and Ground Connections

Pin Name	Pin	Type	Description	Supply
VP2V5A	25, 31, 36, 42	Power	Analog power for ADC.	2.5 V
VP2V5D	28, 39	Power	Digital power for ADC.	2.5 V
VP2V5_SLICER	49	Power	Analog power for SOG Slicer.	2.5 V
VP1V0_PLL	53	Power	Power for LLPLL.	1.0 V
VCC10_TPLL	54	Power	Power for TCI PLL.	1.0 V
AVCC_PLL	12	Power	Analog power for HDMI/MHL TX PLL.	1.0 V
AVCC	4, 9	Power	Digital power for HDMI/MHL TX.	1.0 V
AVCC3V3_CBUS	1	Power	Analog power for CBUS.	3.3 V
CVCC10	13, 60, 65, 69, 82	Power	Power for Digital Core.	1.0 V
VDDIO33	14, 67, 78	Power	Power for Digital I/O.	3.3 V
XTALVCC33	55	Power	Power for XTAL.	3.3 V
XTALGND	58	Ground	Ground for XTAL.	0 V
AVSS	88	Ground	Ground for CBUS.	0 V

6.2.7. Crystal Pins

Pin Name	Pin	Type	Direction	Description
XTALIN	56	Analog	I	Input for Crystal.
XTALOUT	57	Analog	O	Output for Crystal.

6.2.8. Reserved Pins

Table 6.7. Reserved Pins

Pin Name	Pin	Type	Description
D22_RSV	68	RSVD	Reserved.
D23_RSV	66	RSVD	Reserved.
D12_RSV	77	RSVD	Reserved.
D13_RSV	76	RSVD	Reserved.
D14_RSV	71	RSVD	Reserved.
D15_RSV	70	RSVD	Reserved.

7. Design Recommendations

7.1. Typical Connections

Representative circuits for applications of the SiI8784 chip are shown in Figure 7.1 and Figure 7.2. For a detailed review of your intended circuit implementation, contact Lattice Semiconductor.

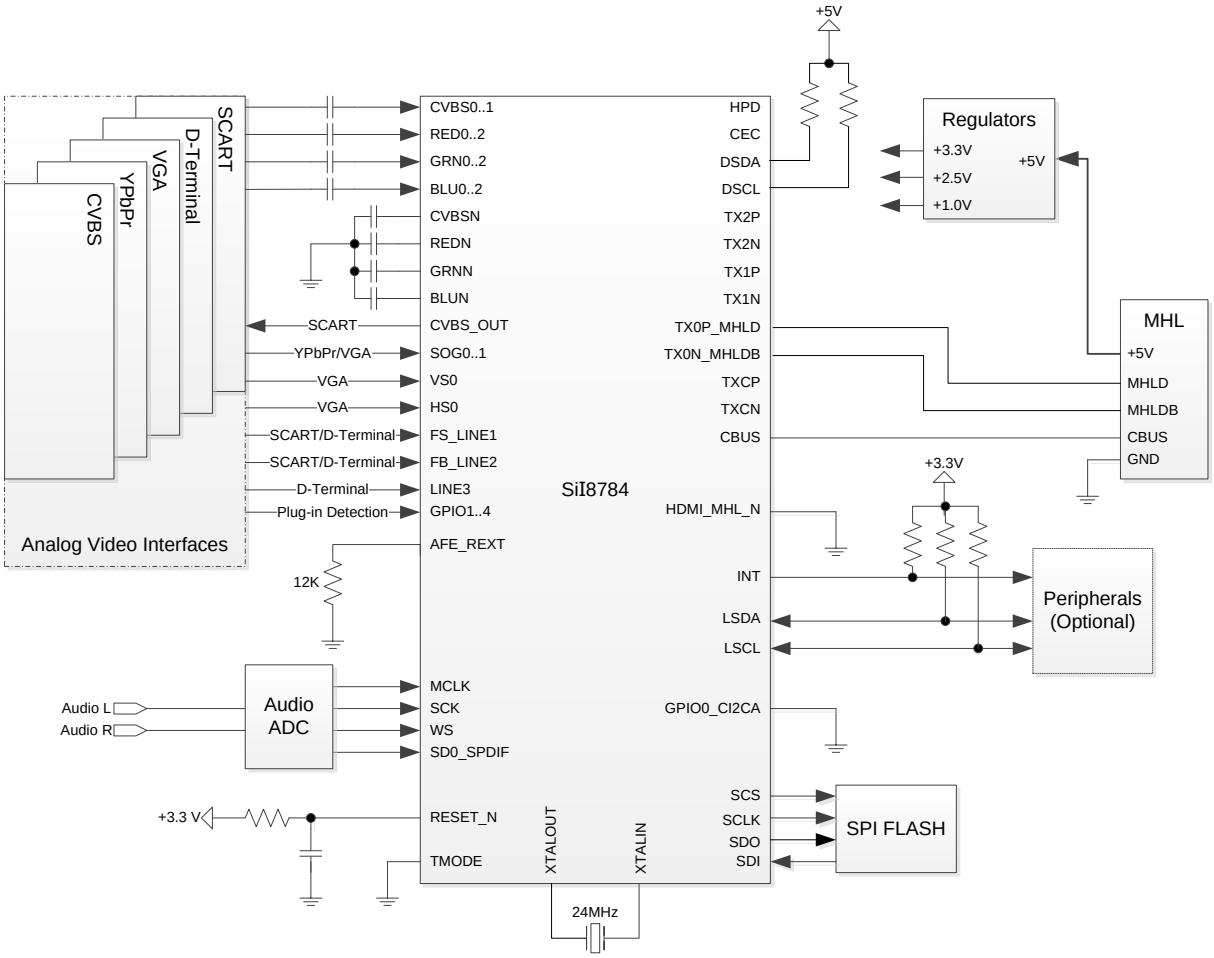


Figure 7.1.Typical Connection Diagram (MHL Output)

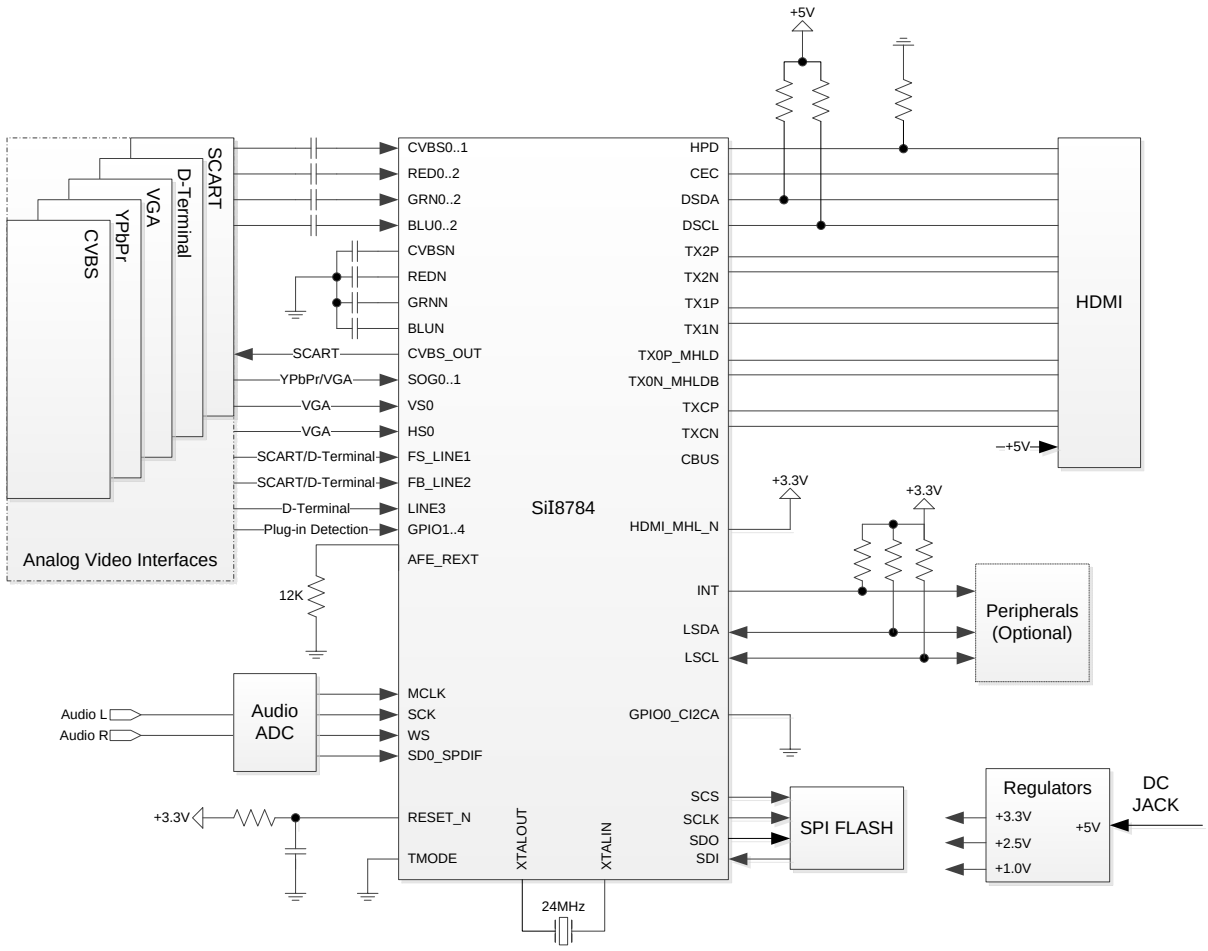


Figure 7.2.Typical Connection Diagram (HDMI Output)

7.2. Power Supplies Decoupling

Designers should include the decoupling and bypass capacitors at each power signal in the layout. These are shown schematically in Figure 7.3. Place these components as close as possible to the input processor differential signals, and avoid routing the differential signals through vias. Figure 7.4 is the representative of the various types of power connections on the input processor.

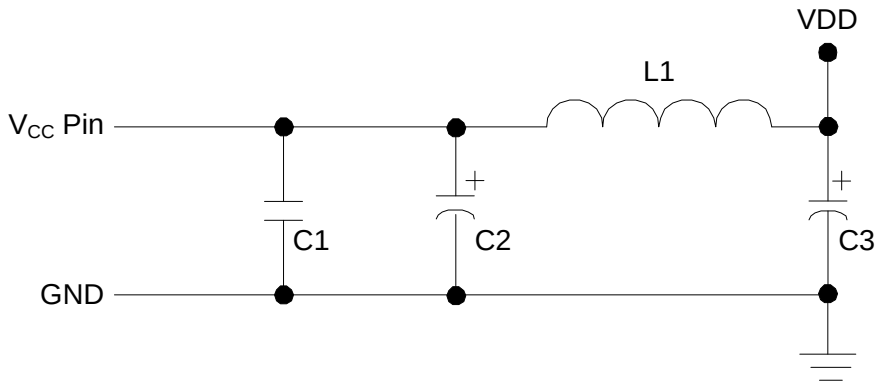


Figure 7.3. Decoupling and Bypass Schematic

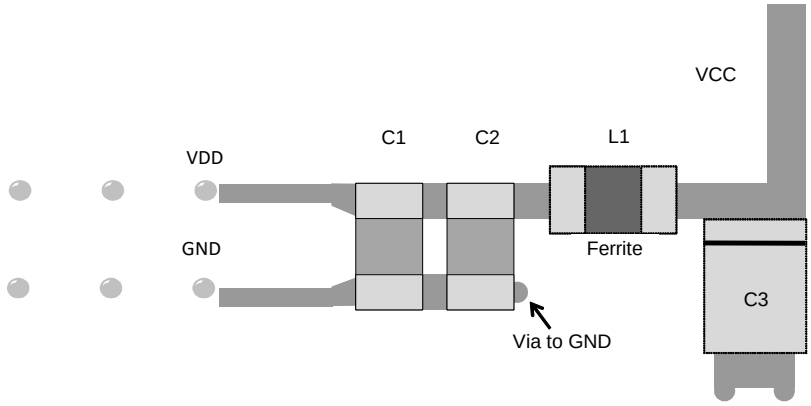


Figure 7.4. Decoupling and Bypass Capacitor Placement

Connections in one group (such as CVCC10) can share C2, C3, and the ferrite, with each ball having a separate C1 placed as close to the ball as possible.

7.3. High-speed HDMI/MHL TMDS Signals

7.3.1. Source Termination

Source termination suppresses the signal reflection and overshoot, and at the same time allows strong input processor drive for longer cable support. The SiI8784 input processor has 100 Ω internal source terminations on the HDMI/MHL differential signal. The common mode clock signal does not have source termination.

7.3.2. ESD Protection

The SiI8784 input processor chip is designed to withstand electrostatic discharge during manufacturing. In applications where higher protection levels are required in the finished product, ESD limiting components can be placed on the differential lines coming out of the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. Use the lowest capacitance devices, if possible. In no case should the capacitance value exceed 1 pF.

7.3.3. Layout Guidelines

The layout guidelines below help to ensure signal integrity. Lattice Semiconductor strongly encourages the board designer to follow the guidelines below.

- Place the input and output connectors that carry the TMDS signals as close as possible to the chip
- Route the differential lines as directly as possible from the connector to the device when using industry-standard HDMI connectors
- Route the two traces of each differential pair together
- Minimize the number of VIAs through which the signal lines are routed
- Layout the MHL input pin traces with a controlled differential impedance of 100 Ω and a common mode impedance of 30 Ω. The differential impedance of the HDMI output pins must be designed within ±15% of 100 Ω
- Serpentine traces are not recommended to compensate for inter-pair trace skew

7.4. EMI Considerations

Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and so on. When attempting to control emissions, do not place any passive components on the differential signal lines (except for the ESD protection and common mode choke described earlier). Lattice Semiconductor recommends the use of a metal shielding can over the SiI8784 chip and the traces going to the connector. The PCB ground plane should extend unbroken under as much of the input processor chip and associated circuitry as possible, with all ground signals of the chip using a common ground.

8. Packaging

8.1. ePad Requirements

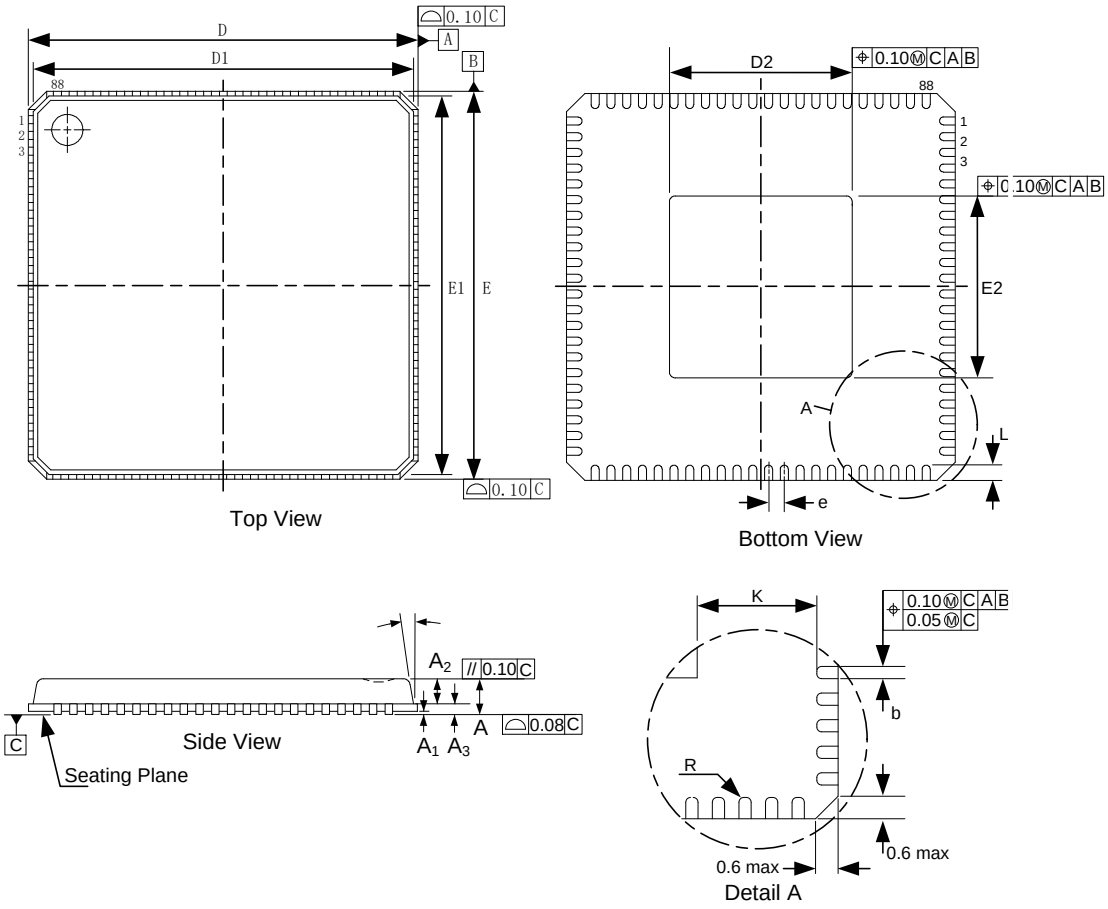
The SiI8784 input processor chip is packaged in 88-pin QFN package with an exposed pad (ePad) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 5.60 mm × 5.60 mm ± 0.15 mm. Soldering the ePad to the ground plane of the PCB is required to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 8.1 on the next page shows the package dimensions of the SiI8784 device.

8.2. Package Dimensions



JEDEC Package Code MO-2206

Item	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A1	Stand-off	0.00	0.02	0.05
A2	Body thickness	0.60	0.65	0.70
A3	Base thickness		0.20 REF	
D	Footprint	9.90	10.00	10.10
E	Footprint	9.90	10.00	10.10
D1	Body size		9.75 BSC	
E1	Body size		9.75 BSC	

Item	Description	Min	Typ	Max
D2	ePad	5.45	5.60	5.75
E2	ePad	5.45	5.60	5.75
b	Lead width	0.15	0.20	0.25
e	Lead pitch		0.40 BSC	
L	Lead foot length	0.30	0.40	0.50
Θ	Mold angle	0°	—	14°
R	Lead radius, inside	0.075	—	—
K	ePad clearance	0.20	—	—

Note: Dimensions in mm.

Figure 8.1. 88-Pin QFN Package Diagram

9. Marking Specification

Figure 9.1 and Figure 9.2 show the markings of the SiI8784 package. These drawings are not to scale.

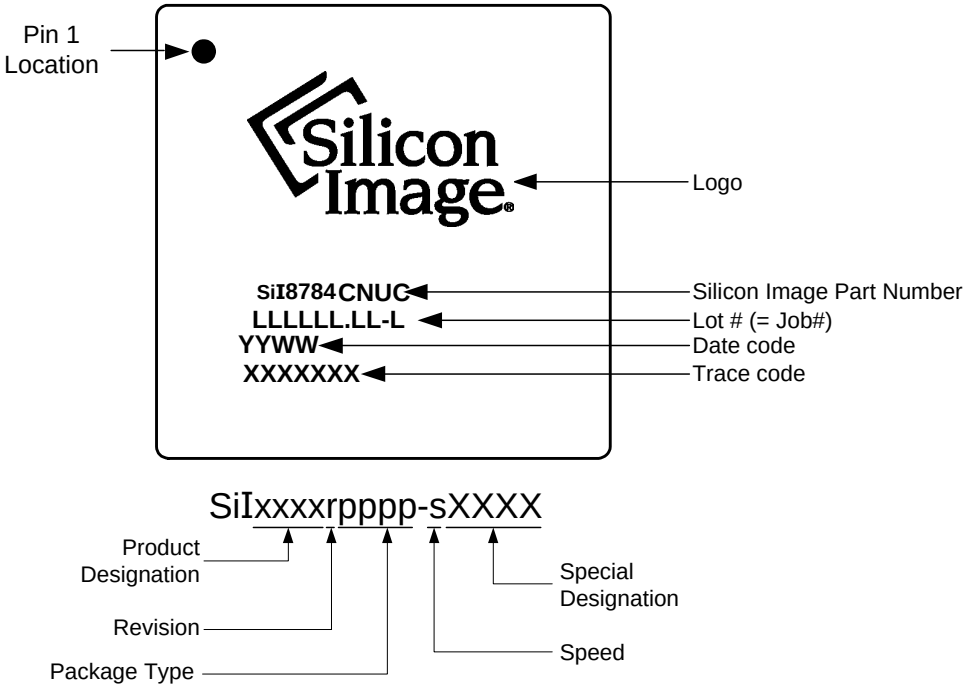


Figure 9.1. Marking Diagram

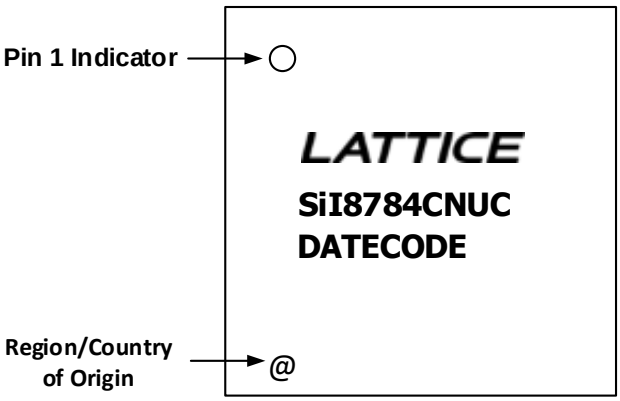


Figure 9.2. Alternate Topside Marking

9.1. Ordering Information

Production Part Numbers:

Device	Part Number
Analog Front End Video Processor with HDMI1.4/MHL2.1 Transmitter	SiI8784CNUC

The universal package can be used in lead-free and ordinary process lines.

References

Standards Documents

This is a list of the standards abbreviations appearing in this document.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface*, Revision 1.4, HDMI Consortium
HCTS	*HDMI Compliance Test Specification,* Revision 1.4, HDMI Consortium.
MHL	*MHL (Mobile High-definition Link) Specification,* Revision 2.1, MHL, LLC.
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.4, Digital-Content Protection, LLC.
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999.
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA; Feb. 2000.
CEA-861-D	*A DTV Profile For Uncompressed High Speed Digital Interfaces*, EIA/CEA; July 2006.
EDDC	*Enhanced Display Data Channel Standard*, Version 1, VESA; September 1999.
I^2C	*The I^2C Bus Specification,* Version 2.1, Philips Semiconductors, January 2000.

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
DVI	http://www.ddwg.org
HDCP	http://www.digital-cp.com
HDMI	http://www.hdmi.org
MHL	http://www.mhlconsortium.org

Lattice Semiconductor Documents

The following are available from your Lattice Semiconductor sales representative. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Document	Title
SiI-AN-0129	*PCB Layout Guidelines: Designing with Exposed Pads*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer's Reference*
SiI-AN-1108	*SiI8784 and SiI8788 Supported SPI Flash Memories*

Revision History

Revision C, June 2017

Figure 9.2. Alternate Topside Marking added per PCN13A16.

Revision B, March 2016

Updated to latest template.

Revision B, September 2014

Summary of changes:

Removed the mentioning of *SiI8784 and SiI8788 Analog Video Process Programmer Reference*.

Details of changes:

Removed the reference to Programmer Reference from Section 3.5.2 Registers, 3.5.4 Interrupt, and Lattice Semiconductor Documents.

Revision A, September 2014

First production release.

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