DESCRIPTION

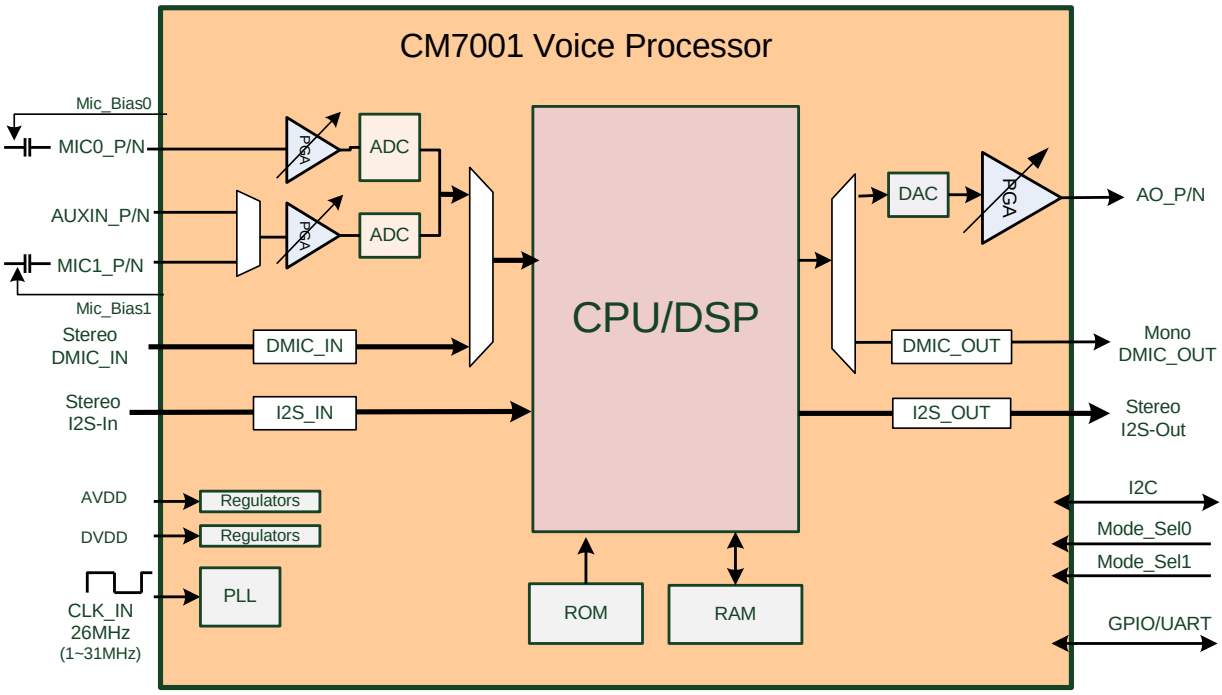
CM7001 is an enhanced and a versatile voice and audio processor system-on-chip (SoC) that is empowered by Cmedia Xear™ sound technologies. For voice communication applications, CM7001 provides Xear™ VoClear close-talk Environmental Noise Cancellation (ENC), far-talk Smart Voice Capture (SVC), Voice Brilliant (HD Voice), AEC, Long Distance Recording (LDR), and Magic Voice for uplink voice sending. It also features Smart Receiver, Noise Reduction, and Voice Brilliant for downlink voice receiving. It could fulfill most communication and voice recognition demands on smartphones, tablets, headsets, speakerphones, smart TV webcam or remote, and a whole lot more. For audio playback applications, CM7001 provides advanced Xear™ Surround Headphone, Sound Expander, and Sonic technologies that dramatically enhances the audio experience of smartphones, tablets, headsets, docking stations and boom boxes. CM7001 is a tiny but powerful voice and audio engine for various applications.

CM7001 is powered by a 32-bit DSP computing core with multiple operation clock and power management options. It integrates all necessary ADC / DAC / Digital Mic / I2S / I2C / PLL / Regulator flexible function blocks and I/O interfaces for easy integration in existing smartphone and embedded platforms.

FEATURES

- World's top performing Xear™ VoClear close-talk ENC and far-talk SVC wideband noise cancellation technologies optimized for voice recognition; Up to 99% (40dB) noise cancellation
- Smart Receiver and Noise Reduction improve receiving voice intelligibility
- Voice Brilliant delivers wideband HD voice experience
- Optimized AEC double-talk performance and far-field Long Distance Recording (LDR) for speakerphones
- Magic Voice transforms voice tones for disguise and/or for fun
- Advanced Xear™ sound technologies and Parametric EQ refresh users' audio experience to both headphones and speakers
- Powerful 32-bit DSP Core with selectable clock speeds
- Analog/Digital microphone I/O interface
- 2-channel I2S I/O interface
- I2C control interface for configuration commands and upgradable F/W
- Two simple Mode_Selector control pins
- Power-Down/Suspend modes for power management
- 30-pin WLCSP (CM7001) / QFN-32 (CM7001N) small footprint packages and pin-compatible with CM7000

BLOCK DIAGRAM



Revision notes

Revision	Date	Description
1.00	2013/05/08	Formal release

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1 Description and overview

Smartphones, tablets, and other portable devices are becoming harder and harder to differentiate from each other. Pursuing only homogeneous HW specification will lead to more rigorous cost and price competition among products. An emergent winning strategy is to add more sensible factors and features to really touch consumers' hearts and satisfy their hidden demands which are not fulfilled or even discovered. Better communication, voice recognition, and audio experience are the greenfield areas that need a seamless, integrated, much better solution to bring customers a really touching user experience. However, it is not an easy job.

C-Media is going after this market trend and is committed to help product makers to realize the innovation in these areas by providing core technologies and component for next generation voice and audio integration solution. In succession to the award-winning CM7000 voice processor SoC, C-Media developed more powerful Xear™ sound technologies on the new CM7001 SoC, not only for voice processing, but also for audio enhancement. Customers could utilize a single chip for equipping versatile and high value-added voice and audio feature set such as:

- More flexible Xear™ VoClear close-talk Environmental Noise Cancellation (ENC) technology achieving up to 99% (40dB) noise cancellation and accommodation of mobile earphone set with in-line microphone applications
- Provides several far-talk Smart Voice Capture (SVC) noise cancellation technologies via dual microphones that have been optimized for voice recognition applications on smartphones, tablets, smart TV remotes, etc.
- Smart Receiver and downlink Noise Reduction improves receiving voice intelligibility and conversation privacy against local dynamic ambient noise level
- Voice Brilliant delivers wideband HD voice experience and ultra voice clarity for both uplink and downlink
- Magic Voice transforms your voice tones for disguise and/or for fun over phones, VoIP, or voice memo applications
- Enhanced and optimized Acoustic Echo Cancellation (AEC) double-talk performance for speakerphone/hands-free applications
- Far-field Long Distance Recording (LDR) could pick up far voice sources of a group conference in a big room for long-range speakerphones, tablets, STBs, webcams, and smart TV applications
- CM7001 exclusive Xear™ Surround and Xear™ Sonic sound technologies could dramatically refresh users' audio experience over both headphones, built-in speakers, or external docking speakers
- Programmable Parametric EQ for sound tuning
- Online and offline Mic Auto-Calibration capability to accommodate two microphones' sensitivity mismatching in the whole product life cycle or in the production line. This feature reduces microphone cost, production efforts, failure rate, and total cost of services. It automatically improves performance stability for each shipped product.

C-Media's amazing Xear™ VoClear Environmental Noise Cancellation (ENC) technology has been well proven as the world's top performing noise canceling and private conversation solution by mobile phone and headset makers. Utilizing the same dual microphone signal capturing, CM7001 voice processor with advance VoClear™ SVC algorithms could effectively capture voice input and isolate the dynamic ambient noises and surrounding voices to improve the voice recognition success rate significantly. All speech processing is running with wideband frequency range for HD voice clarity. It would be a necessary complementary component for voice recognition front-end input devices.

With CM7001 Xear™ VoClear solution built into smartphones, users need not to worry about their calling places or repeating their words loudly. It could enhance conversation convenience, receiving speech intelligibility, privacy, and voice recognition accuracy. Hence, it will deliver a better than ever speech application user experience. In addition, CM7001's Xear™ audio technologies could create a tailor-made, whole new 3D surround, deep bass, brilliant, true-to-life and convenient audio experience of music, video and games, breaking through the physical limitations of earphones or tiny speakers for a variety of products, such as smartphones, tablets, docks, speakers, boom boxes, portable players, headsets, etc.

CM7001 is a highly-integrated, mixed-signal system-on-chip (SoC) voice and audio processor, powered by a 32-bit DSP computing core with multiple operation clock and power management options. It integrates all necessary ADC / DAC / Digital Mic / I2S / I2C / PLL / Regulator flexible function blocks and I/O interfaces for easy integration in existing smartphone and embedded platforms. Moreover, CM7001 flexibly allows customers to fine-tune and customize abundant algorithm parameters or even to download new F/W codes via simple I2C programming interface from an application processor/baseband/MCU or an external EEPROM to build the best solution for their own products. It will come with an ease-of-use PC configuration tool and Android SDK/sample codes. With very compact WLCSP 30 balls

(CM7001, 2.625 x 2.998 mm) and QFN-32 package (CM7001N, 5 x 5 mm) ordering options and fully pin-compatible with CM7000/CM7000N, CM7001/CM7001N would be the best and the fastest solution to implement a powerful, one-for-all voice and audio solution that offloads voice and audio processing from the host application processor and saves overall system power consumption. CM7001, as small footprint as CM7000 but has far more powerful features, is a high-value voice and audio DSP engine in a single SoC for consumer products.

1.1 Functions:

Technology/Functions	Microphones Required	Application Scenarios
ENC (Environmental Noise Cancellation)	Dual-mic	Handset conversation, voice-command
AEC (Acoustic Echo Cancellation)	Mono-mic	Speakerphone, videophone, hands-free, voice-command
NR (Noise Reduction)	Mono-mic	Camcorder, voice recorder, plug-in headset, voice-command
SVC (Smart Voice Capture)	Dual-mic	Hands-free, gaming, voice-command, interview, pen-recorder
LDR (Long Distance Recording)	Dual-mic	Speakerphone, videophone, hands-free, voice-command
Smart Receiver(Downlink)	Mono-mic	Handset conversation
Voice Brilliant(HD Voice, Up/Downlink)	Mono-mic	Handset conversation, speakerphone
Magic Voice(Uplink)	Mono-mic	Handset conversation, speakerphone
Surround Headphone		Music playback with sound effect
Sound Expander		Music playback with sound effect
Dynamic Bass		Music playback with sound effect
Audio Brilliant		Music playback with sound effect
Smart Volume		Music playback with sound effect
Parametric EQ		Music playback with sound effect

2 Ordering information

Product	Package Marking	Package Type	Transport Media	Storage Temperature
CM7001	CM7001	WLCSP-30 (2.625 x 2.998mm) green package	Tape & Reel	-45 to 120℃
CM7001N	CM7001N	QFN-32 (5 x 5 mm) green package	Tray	-45 to 120℃

3 Features

3.1 Algorithms

- Features Xear™ VoClear Environment Noise Cancellation (ENC) technology for dual omni-microphones
- Adjustable 20-40dB cancellation of environmental dynamic and stationary noises and other parameters
- Supports a mic auto-calibration mechanism, allowing dual-mic sensitivity and mismatching in production
- Allows a wide placement distance range between two microphones (8-14 cm recommended)
- Supports mic-in auto-gain control (AGC) for ADC recording quality when the ENC function is on
- Optional Acoustic Echo Cancellation (AEC) processing mode for speakerphones
- Far-Talk SVC (Smart Voice Capture) to capture unidirectional voice
- Optional mono-mic noise reduction (NR) processing mode for camcorder/voice recorders
- Long Distance Recording (LDR) to capture voice clearly and without distortion within 5 m area
- Smart Receiver automatically optimizes downlink voice volume in relation to the local background noise level
- Voice Brilliant to enhance voice clarity for downlink and uplink
- Magic Voice to transform your voice tones for disguise and/or for fun
- Xear™ Surround Headphone creates a realistic 3D surround sound field over stereo headphones
- Xear™ Dynamic Bass reproduces deep and vibrating bass in music, movies, and games even while using a small speaker/headphone drivers and enclosures
- Xear™ Audio Brilliant restores clarity and details of compressed audio in music, movies, and games (MP3, WMA, AAC, AC3, etc.), making sound more dynamic and brilliant
- Xear™ Smart Volume normalizes overall perceptual sound levels for different music, games, Internet AV clips, and movies
- 5-band parametric EQ
- 16-bit/16kHz high-fidelity voice processing

3.2 SoC architecture

- 32-bit DSP core
- Selectable DSP operating clock speeds
- 120k-byte ROM
- 32k-byte data RAM
- 36k-byte instruction RAM
- Single clock source required with internal PLL (1~31MHz configurable and flexible clock architecture)

3.3 Audio/Voice I/O

- Dual differential analog microphone inputs (default path)
- Two microphone bias voltage pins (default ON)
- Mono differential analog output (default path)
- Configurable digital microphone PDM input/output interface
- Configurable 2-channel I2S digital input/output interface (slave mode, I2S/left-justified)
- I2S supports 16/24/32-bit and multiple sample rates from 8K ~192kHz
- Supports differential analog aux-in for AEC-function speaker reference signal input

- Supports flexible I/O connection and configurable signal routing paths by internal ROM codes:
  - analog-to-analog (default)
  - DMIC-to-DMIC
  - I2S-to-I2S
  - analog-to-I2S
  - DMIC-to-I2S
- Allows by-passing DSP process from inputs to outputs

3.4 Control interface

- Supports 2-mode selector control input pins, or I2C control to switch among 4 chip operation modes: Power-Down/Active /Bypass/Suspend
- Master/slave I2C control interface for interaction with the baseband, application processor, MCU, EEPROM, or other components (supports 100kHz and 400kHz speeds; 100kHz is the default in master mode)
- Configurable UART control interface
- Supports up to 8 GPIOs (shared pins)

3.5 Power management

- Supports 4-power state/operation modes: Power-down/Active/Bypass/Suspend
- Power-down mode current (for power saving in standby/sleep states of mobile phones): < 1uA
- Active mode current (ENC-ON): ~21.16 mA (AVDD=2.8V, DVDD=1.8V, Clock=26 MHz, digital mic in/out)
- Supply current can be lower with some advanced power management configurations
- Wide power supply range with built-in LDO regulators

3.6 Audio DAC/ADC

- Embedded 2-channel audio sigma-delta ADC
- Embedded mono audio DAC
- 16-bit/16kHz high-fidelity voice data conversion
- High S-N ratio: ~90 dB
- Supports mic pre-ampilifer with PGA gain: 0~+31dB, 1dB/step (default=+20dB)
- Aux-In PGA gain: -12~+19dB, 1dB/step (default=+8dB)
- Supports DAC PGA gain: 0 ~ -31dB, 1dB/step (default= -17dB)

3.7 F/W control

- Allows the baseband to read/write commands/parameters in RAM or HW registers via I2C in real-time
- Allows downloads to upgrade the entire F/W codes into instruction RAM via I2C
- Power-on loading F/W codes or customized HW and algorithm parameters from external I2C EEPROM\

3.8 Miscellaneous

- 3.3V tolerance digital I/O
- Two small footprint package options:
  - CM7001: 30-balls WLCSP small footprint green package (5 x 6 balls, 2.625 x 2.998mm, 0.5mm pitch)
  - CM7001N: QFN-32 pin green package (5 x 5mm)

4 Applications

- Smartphones
- Mobile featured phones
- DECT/PSTN/VoIP phones
- Bluetooth headsets
- USB headsets/handsets
- Battery-powered headset/wireless headsets
- Speakerphone
- Array mic
- Docking with sound effect

5 Block diagram

Figure 5.1 shows an internal block diagram of the CM7001 voice processor. Featuring a neat design, it makes an ideal voice capturing and noise canceling pre-processor capable of fitting into the microphone input path or digital I2S input path of any type of communication device. As an added benefit, traditional and original microphone input circuitry and components do not need to be changed much.

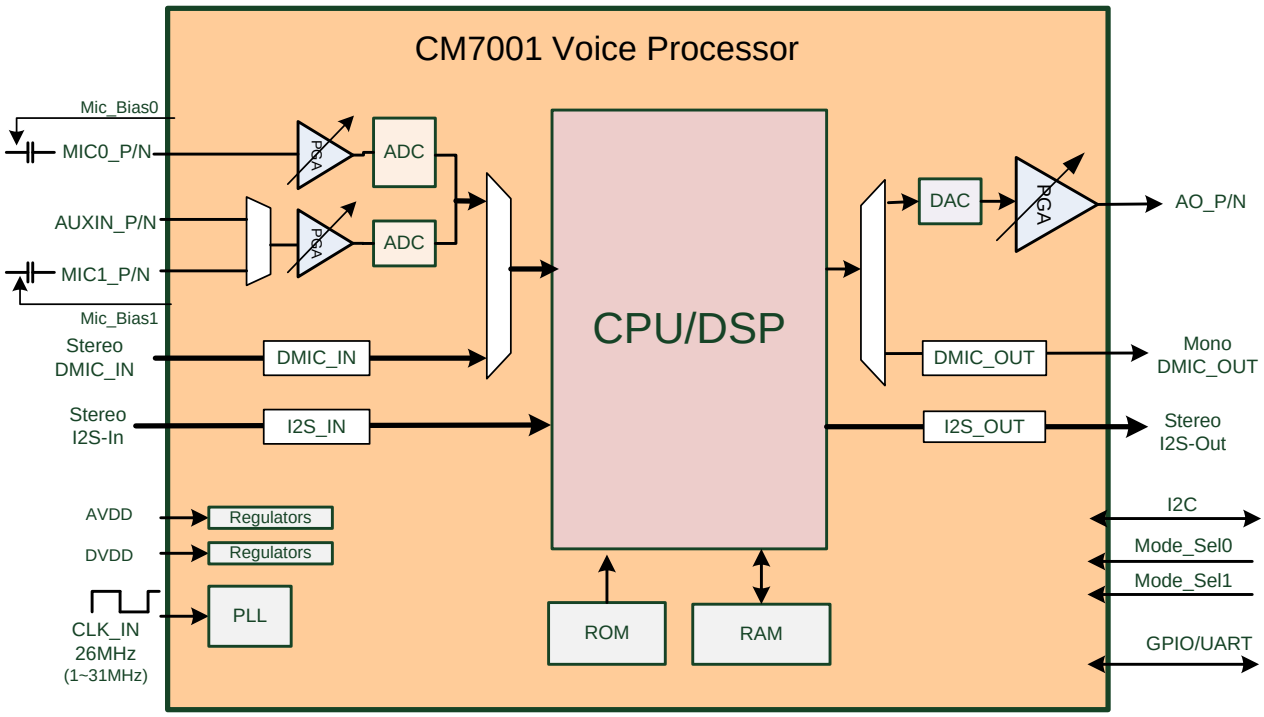


Figure 5.1 CM7001/CM7001N Functional Block Diagram

6 Pin assignment

6.1 Pin-out diagram

CM7001 Top View (WLCSP 30-Ball 5x6, 2.625 x 2.998 mm)

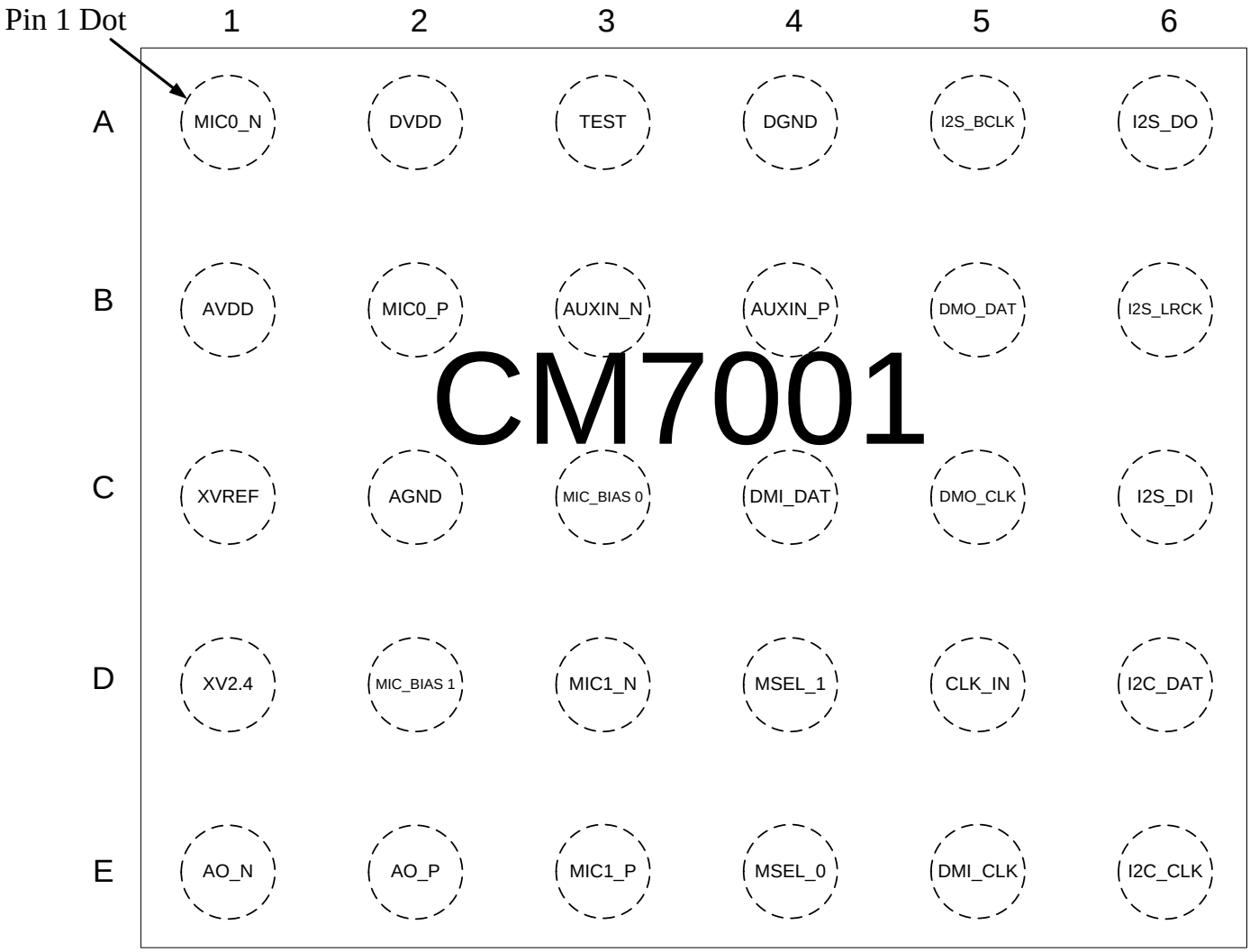


Figure 6.1 CM7001 Pin-out Diagram (Top View)

CM7001 Bottom View / Ball Side (WLCSP 30-Ball 5x6, 2.625 x 2.998 mm)

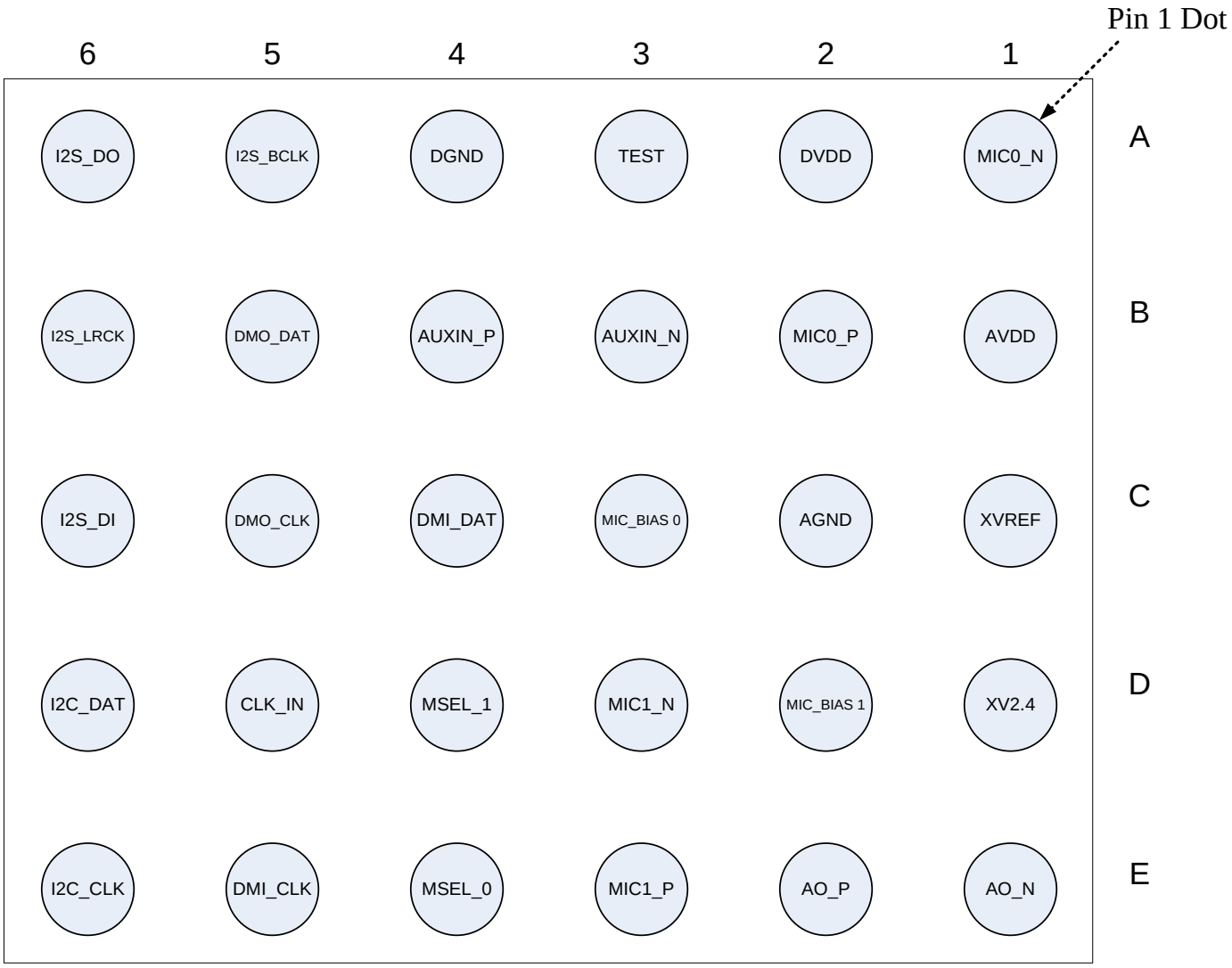


Figure 6.2 CM7001 Pin-out Diagram (Bottom View)

CM7001N Top View (QFN-32 5x 5 mm)

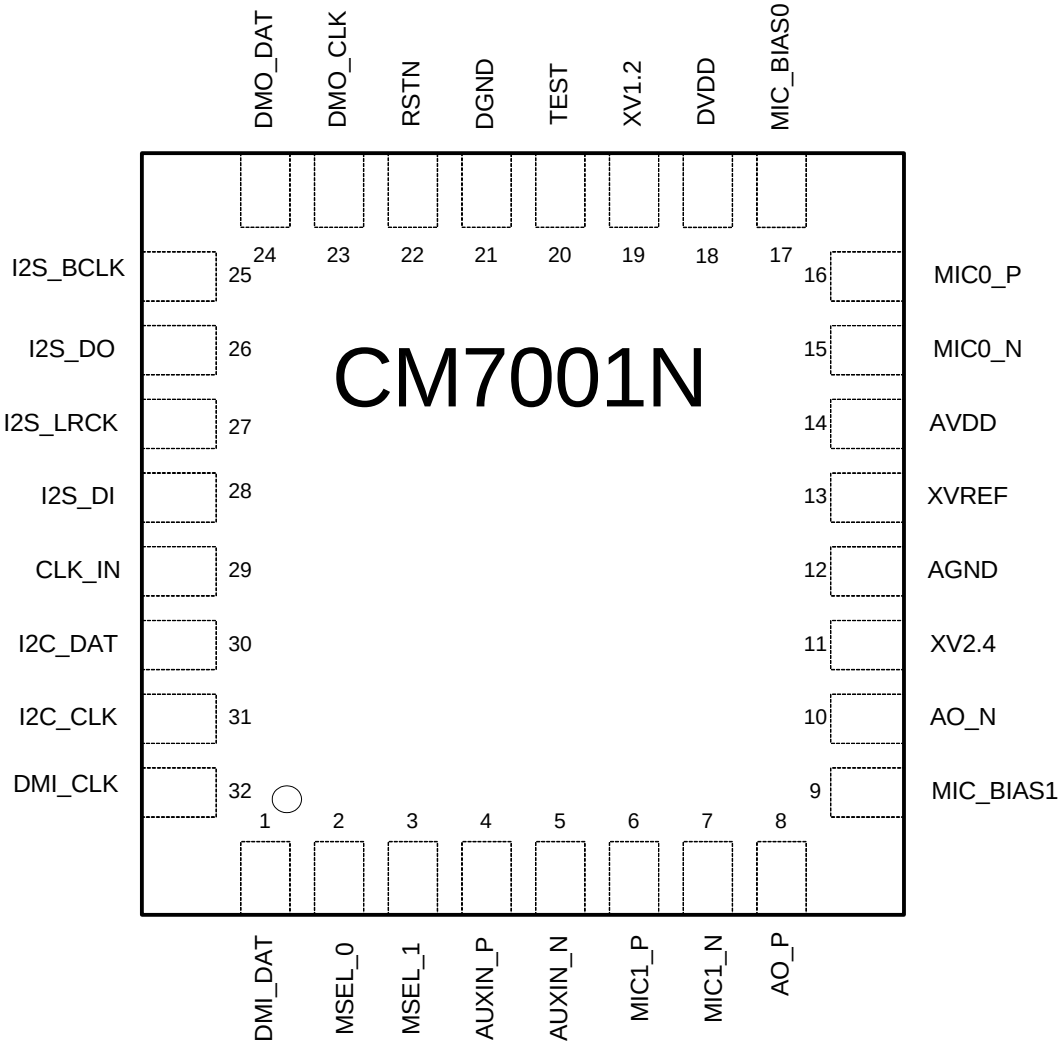


Figure 6.3 CM7001N Pin-out Diagram (Top View)

6.2 Pin description

CM7001 Pin Description (WLCSP 30-Ball 5x6)

Pin #	Symbol	I/O	Description
Clock Input			
D5	CLK_IN	DI, PD	Clock input (default 26MHz, configurable from 1~31MHz)
Power/Ground			
B1	AVDD	PWR	Analog power
A2	DVDD	PWR	Digital power
D1	XV24	AIO	Regulator capacitor filter for analog circuit
C1	XVREF	AO	Voltage reference capacitor filter
C2	AGND	PWR	Analog ground
A4	DGND	PWR	Digital ground
C3	MIC_BIAS0	AO	Bias voltage: 1.9V for microphone 0
D2	MIC_BIAS1	AO	Bias voltage: 1.9V for microphone 1
Digital Interface			
E4	MSEL_0	DI, PD1	Model selector pin 0
D4	MSEL_1	DI, PD1	Model selector pin 1; Mode selector Values (pin 1, pin0): 0x00: power down (default) 0x01: active (ENC ON) 0x11: by-pass mode (Effect Off) 0x10: suspend
E5	GPIO0 / DMI_CLK / I2SR _BCLK	DIO, PD	GPIO0 (default, input) Digital microphone clock output I2S recording bit clock
C4	GPIO1 / DMI_DAT / I2SR _LRCK	DIO, PD	GPIO1 (default, input) Digital microphone data input I2S recording left/right clock
C5	GPIO2 / DMO_CLK	DIO, PD	GPIO2 (default, input) Digital microphone clock input
B5	GPIO3 / DMO_DAT	DIO, PD	GPIO3 (default, input) Digital microphone data output
A5	GPIO4 / I2S _BCLK	DIO, PD	GPIO4 (default, output) I2S playback bit clock
B6	GPIO5 / I2S _LRCK	DIO, PD	GPIO5 (default, input) I2S playback left/right clock
A6	TXD / I2S_DO GPIO6	DIO, PD	UART transmit I2S serial data output GPIO6
C6	RXD / I2S_DI / GPIO7	DIO, PU	UART receive (internal pull-up in active mode) I2S serial data input GPIO7

E6	I2C_CLK	DIO, PU	I2C clock
D6	I2C_DAT	DIO, PU	I2C data
Analog Interface			
B2	MIC0_P	AIN	Differential analog microphone 0 input P
A1	MIC0_N	AIN	Differential analog microphone 0 input N
E3	MIC1_P	AI	Differential analog microphone 1 input P
D3	MIC1_N	AI	Differential analog microphone 1 input N
B4	AUXIN_P	AI	Differential analog aux line input P
B3	AUXIN_N	AI	Differential analog aux line input N
E2	AO_P	AO	Differential analog output P
E1	AO_N	AO	Differential analog output N
Miscellaneous			
A3	TEST	DI, PD	Test mode enable, high active

NoteU:
1. DI/DO/DIO-Digital Input/Output/Bi-Directional Pad
2. AI/AO/AIO-Analog Input/Output/Bi-Directional Pad
3. PD/PD1-Pull Down (PD~75K Ohms/PD1~500K ohms)
4. PU- Pull Up ~75Kohms

CM7001N Pin Description (QFN-32)

Pin #	Symbol	I/O	Description
Clock Input			
29	CLK_IN	DI, PD	Clock input (default 26MHz, configurable for 1~31MHz)
Power/Ground			
14	AVDD	PWR	Analog power
18	DVDD	PWR	Digital power
11	XV2.4	AIO	Regulator capacitor filter for analog circuit
19	XV1.2	AIO	Regulator capacitor filter for digital and PLL circuit (for CM7001N only)
13	XVREF	AO	Voltage reference capacitor filter
12	AGND	PWR	Analog ground
21	DGND	PWR	Digital ground
17	MIC_BIAS0	AO	Bias voltage 1.9V for microphone 0
9	MIC_BIAS1	AO	Bias voltage 1.9V for microphone 1
Digital Interface			
2	MSEL_0	DI, PD1	Model selector pin 0
3	MSEL_1	DI, PD1	Model selector pin 1; Mode selector values (pin 1, pin0): 0x00: power down (default) 0x01: active (ENC ON) 0x11: by-pass mode (effect off) 0x10: suspend
32	GPIO0 / DMI_CLK / I2SR _BCLK	DIO, PD	GPIO0 (default, input) Digital microphone clock output I2S recording bit clock

1	GPIO1 / DMI_DAT I2SR _LRCK	DIO, PD	GPIO1 (default, input) Digital microphone data input I2S recording left/right clock
23	GPIO2 / DMO_CLK	DIO, PD	GPIO2 (default, input) Digital microphone clock input
24	GPIO3 / DMO_DAT	DIO, PD	GPIO3 (default, input) Digital microphone data output
25	GPIO4 / I2S _BCLK	DIO, PD	GPIO4 (default, output) I2S playback bit clock
27	GPIO5 / I2S _LRCK	DIO, PD	GPIO5 (default, input) I2S playback left/right clock
26	TXD / I2S_DO GPIO6	DIO, PD	UART transmit I2S serial data output GPIO6
28	RXD / I2S_DI / GPIO7	DIO, PU	UART receive (internal pull-up in active mode) I2S serial data input GPIO7
31	I2C_CLK	DIO, PU	I2C clock
30	I2C_DAT	DIO, PU	I2C data
Analog Interface			
16	MIC0_P	AIN	Differential analog microphone 0 input P
15	MIC0_N	AIN	Differential analog microphone 0 input N
6	MIC1_P	AI	Differential analog microphone 1 input P
7	MIC1_N	AI	Differential analog microphone 1 input N
4	AUXIN_P	AI	Differential analog aux line input P
5	AUXIN_N	AI	Differential analog aux line input N
8	AO_P	AO	Differential analog output P
10	AO_N	AO	Differential analog output N
Miscellaneous			
20	TEST	DI, PD	Test mode enable, high active
22	RSTN	DI, PU	Chip reset input, low active (for CM7001N only)

Notes:
1. DI/DO/DIO-Digital Input/Output/Bi-Directional Pad
2. AI/AO/AIO-Analog Input/Output/Bi-Directional Pad
3. PD/PD1-Pull Down (PD~75K ohms/PD1~500K ohms)
4. PU- Pull Up ~75K ohms

7 Functional description

7.1 Operation modes

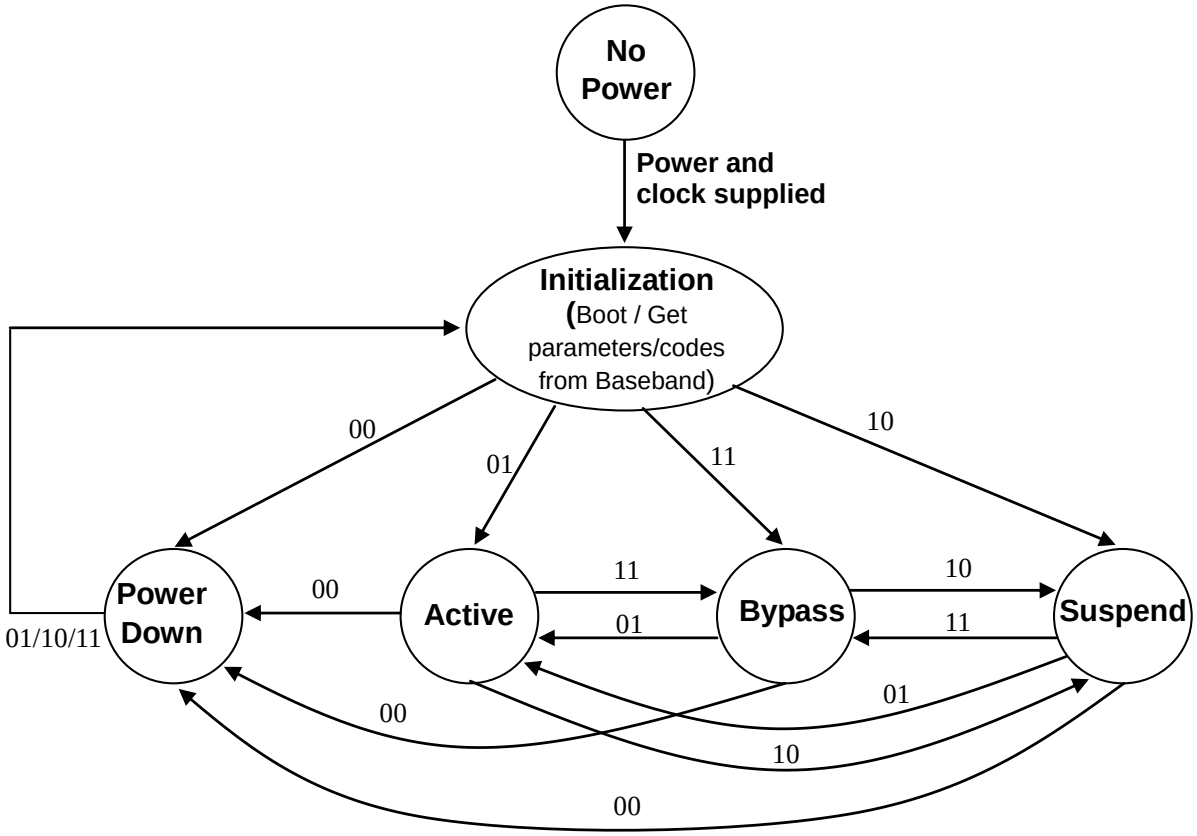
The CM7001 supports 4 operation modes with different power management levels for easy operational control, including power-down, Algorithm on, bypass, and suspend modes. These modes can be controlled by 2 HW mode_selector input pins (default setting), or by I2C command control set from the host controller/baseband. When the I2C is chosen to switch these modes, then the DSP receives the mode-switch command from the baseband chip through the I2C interface and writes the result to the 2-bit mode_sel registers to handle mode/power control. If the baseband chip chooses the I2C interface to control the mode selection, then some of the CM7001 function blocks will be kept alive while in suspend and power-down modes.

Mode_Sel Pins Register[1:0]	Mode	Description
00	Power Down (default)	Default state mobile device power-saving standby mode, sleep, deep-sleep, or power-off states
01	Active (algorithm on)	List all algorithm Chip and voice processor is turned on for active state (calling). ENC is the default function, host CPU can switch the function to AEC or NR for different applications via I2C commands.
11	Bypass(algorithm off)	Bypass voice process and Audio effect redirect mic-in signals to mic-out directly (an option allowing users to turn off ENC/AEC/NR functions during calls or other applications)
10	Suspend	Reserved alternative suspend mode in phone's standby or sleep states, especially for keeping new downloaded F/W codes in the internal RAM, saving the reloading time for ENC- On

7.2 Mode state diagram and power management

The following diagrams illustrate mode switch states and corresponding power levels (level 0-4) for Mode_Sel and the I2C interface respectively.

Mode State Diagram Controlled by Two Mode_Sel (1,0) Pins



Power Down Mode—
- Digital power level 0: No power
- Analog power level 0: Minimum analog power consumption

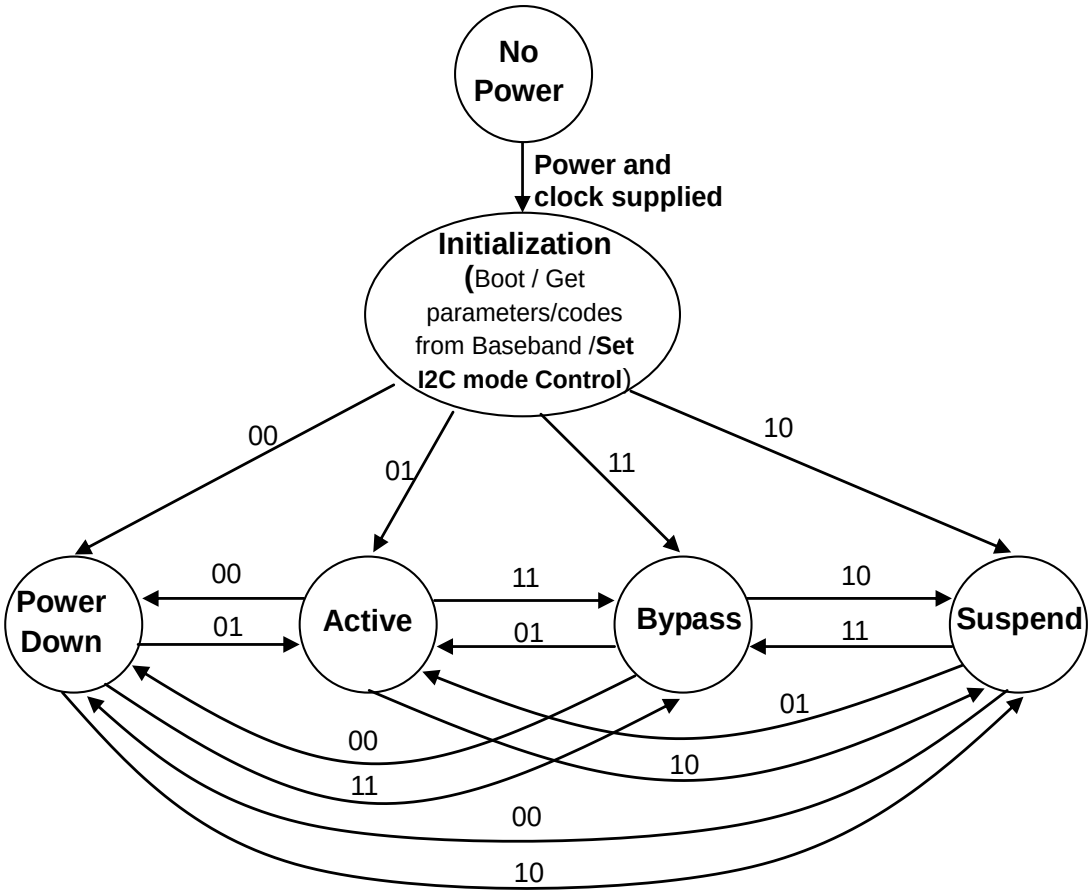
Active Mode—
- Digital power level 4: Normal operation
- Analog power level 4: Normal operation

Bypass Mode—
- Digital power level 3: By-pass DSP core processing
- Analog power level 4: Normal operation

Suspend Mode—
- Digital power level 1: Digital core only consume static power
- Analog power level 1: Analog keeps digital core LDO voltage on

Figure 7.1 Mode State Diagram (by Mode_Sel pins)

Mode State Diagram Controlled by I2C Bus



Power Down Mode—
- Digital power level 2: DSP core is operated at a lowest frequency
- Analog power level 2: Analog keeps digital core/PLL LDO voltages on

Active Mode—
- Digital power level 4: Normal operation
- Analog power level 4: Normal operation

Bypass Mode—
- Digital power level 3: By-pass DSP Core processing
- Analog power level 4: Normal operation

Suspend Mode—
- Digital power level 2: DSP core is operated at a lowest frequency
- Analog power level 2: Analog keeps digital core/PLL LDO voltages on

Figure 7.2 Mode State Diagram (by I2C interface)

7.3 Recommended control methods

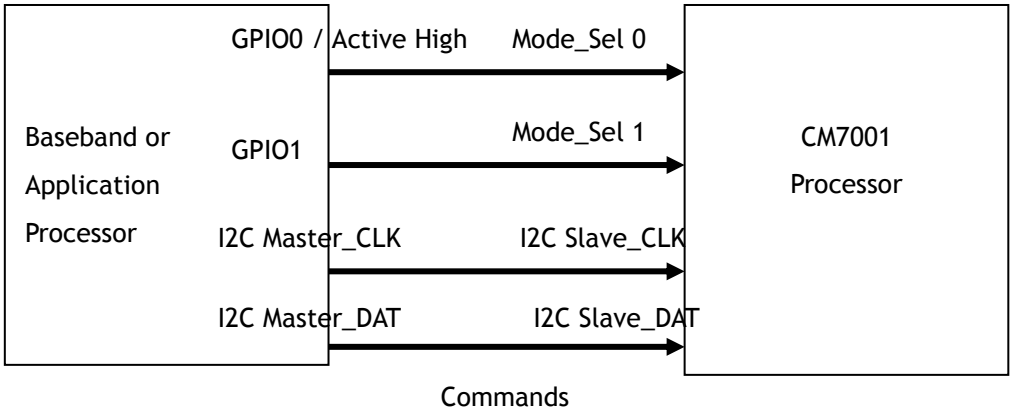
There are three recommended control scenarios for different customer considerations:

Mode_Sel pin control for non-custom tuning or programming parameters with the best power savings

In typical cases, if you need to change some ROM code parameters or set HW registers via the I2C interface, we recommend using Mode_Sel 0/1 pins to easily control the chip operation mode for improved power savings. In this way, the power-down mode will be changed to power level 0, consuming almost no power when on standby/sleep/deep-sleep or power-off modes. During a call, when the phone is active, it will switch to ENC mode via baseband's active signal pin or a GPIO pin (drive high) to Mode_Sel0 pin. When pulled down, this pin will power-down the phone when a call is ended, returning it to standby status. Another GPIO pin can drive Mode_Sel1 pin high (while Mode_Sel 0 is high at the same time) to enter bypass mode when the user chooses to turn off the ENC function, or if the phone design does not allow it to use the CM7001's AEC or NR functions in speakerphone and recorder applications. The phone status should match the following operation modes:

Phone Status	Power-Off	Stand-By/Sleep/ Deep-sleep	Active (Effect On)	Active (Effect Off)
Operation mode	Power down (no power supply)	Power down	Active (Algorithm on by I2C command)	Bypass
Mode_Sel0/1 control	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=1

In this scenario, please note that the baseband needs to program the parameters or HW registers through the I2C every time before entering into phone active/calling status with the ENC chip working (very-short time of ~0.12ms).

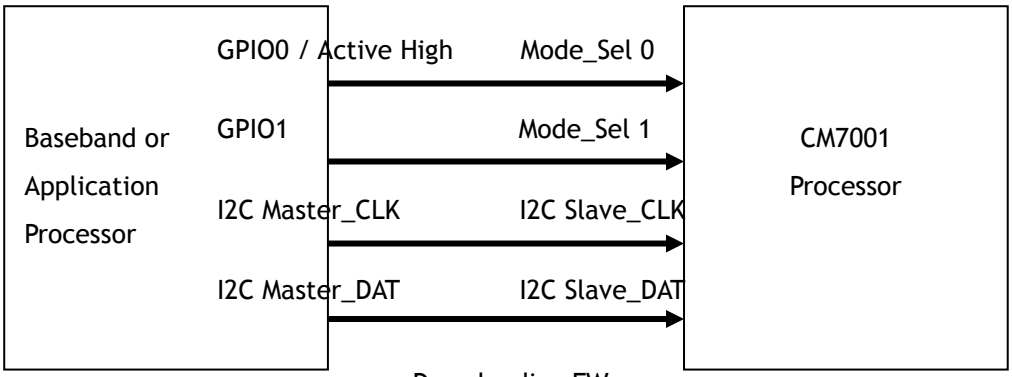


Mode_Sel pin control for demand to download firmware codes with power saving

When the default DSP algorithm ROM codes CANNOT satisfy your needs, the CM7001 ENC chip allows the baseband to download a whole new version of codes into the program's RAM through the I2C interface. In this situation, we still recommend using Mode_Sel 0/1 pins to easily control the chip's operation mode for better power saving. However, to avoid downloading times (1.16 sec for 32Kbytes FW @ I2C fast mode) every time the phone comes out of power-down mode, it might be necessary to use the suspend mode (Mode_Sel0=low, Mode_Sel1=high) for phone standby or sleep status settings, which will keep the RAM program/data operational.

When the phone is active during a call, switch to active ENC-On mode via the baseband's phone active signal pin or a GPIO pin (Mode_Sel0 pin must be pulled high and the Mode_Sel1 pin must be pulled low at the same time. The reverse position puts the phone back in standby/sleep mode). Just like scenario one, drive both Mode_Sel 0/1 pins to high at the same time to enter by-pass mode when the user wants to turn off ENC for calls. Again, the phone status should match the following operation modes:

Phone Status	Power-Off/ Deep-Sleep	Stand-By/Sleep	Active (Effect On)	Active (Effect Off)
Operation mode	Power down (no power supply)	Suspend	Active (Algorithm on by I2C command)	Bypass
Mode_Sel0/1 control	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=0 Mode_Sel 1=1	Mode_Sel 0=1 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=1



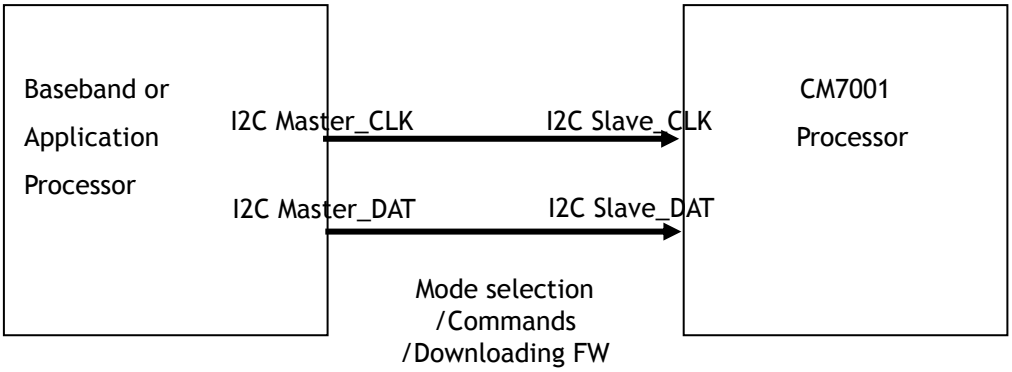
Downloading FW

I2C-only Control Scenario

The CM7001 chip also allows the baseband to switch operation modes via I2C programming hardware registers if customers do not want to use additional GPIO control. This means that only the I2C controls the ENC chip, necessitating higher power levels to keep the I2C slave interface and digital core alive the device is on standby. In this situation, we recommend using the power-down (00) or suspend (10) mode for the phone standby status (in this scenario, these modes are actually the same), which will keep the RAM program/data and I2C operation.

Therefore, the baseband does not need to program or download codes every time the phone becomes active for calls. Set registers [1:0] as 01 are used for ENC-On operation while the unit is in operation. It goes back into power down/suspend mode when the call is ended and returns to standby/sleep status. Just like scenarios one and two, set registers [1:0] as 11 are used to enter bypass mode when the user would like to turn off ENC for calls or other applications. The phone status should match the following operation modes via I2C interface writing from the baseband:

Phone Status	Power-Off	Stand-By/Sleep/ Deep-sleep	Active (Effect On)	Active (Effect Off)
Operation mode	Power down (no power supply)	Power down or suspend	Active (algorithm on by I2C command)	Bypass
Mode_Sel0/1 control	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=0 Mode_Sel 1=0 or 1	Mode_Sel 0=1 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=1



8 Electrical characteristics

8.1 Absolute maximum ratings

Parameter	Symbol	Min	Max	Units
Storage temperature	Ts	-45	120	°C
Operating ambient temperature	T_A	-25	70	°C
Analog supply voltage	AVDD	2.2[1]	3.6	V
Digital supply voltage	DVDD	1.65	3.6	V
Digital input voltage	-	-0.3	DVDD	V
ESD (HBM)	-	4KV	-	V
ESD (MM)	-	200	-	V
Latch-up	-	200	-	mA

Note：In default analog codec mode, AVDD needs to be >=2.2V to make internal codec work properly.

8.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Units
Storge temperature	T_S	-	25	-	°C
Operating ambient temperature	T_A	-	25	-	°C
Analog supply voltage (AVDD)	AVDD	2.4[1]	2.8	3.6	V
Digital supply voltage (DVDD)	DVDD	1.65	1.8/2.8	3.6	V
Digital input voltage	-	0	DVDD	DVDD+0.3	V
Clock source	CLK_IN	1	26[2]	31	MHz
Clock source accuracy	-	-	50		ppm

Notes：

1. In default analog codec mode, AVDD is recommended to be >=2.4V to allow the internal codec to work properly and achieve the best audio quality.
2. 26MHz is a default assumption for clock source, but other common clock sources on mobile phones, like 13MHz and 19.2MHz, are also compatilbe with proper PLL frequency divider setting.

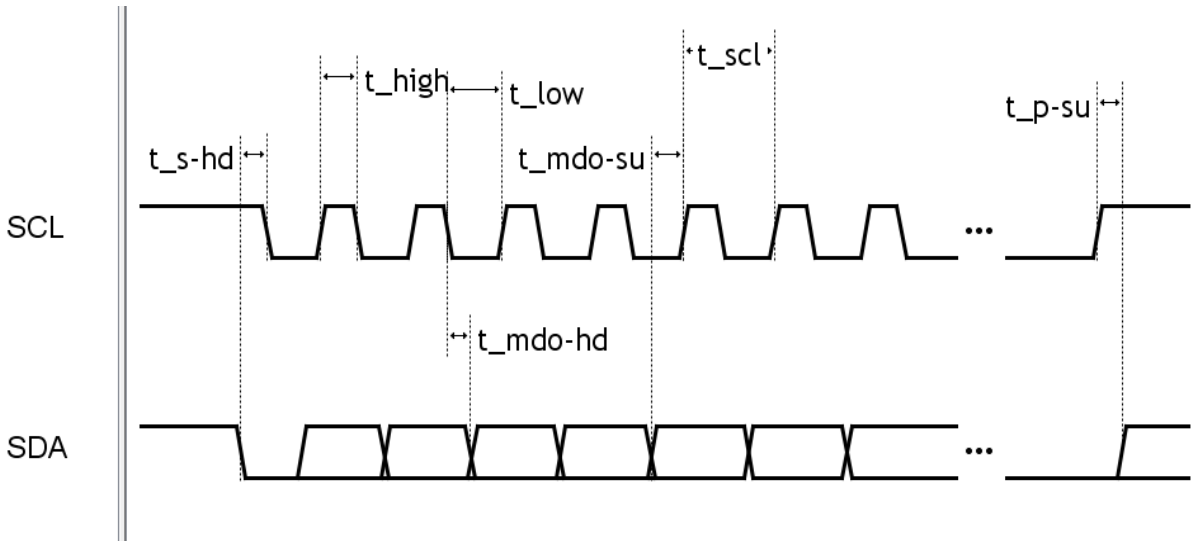
8.3 DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
High level input voltage	Vih	0.7*DVDD[1] (DVDD<=2.8V) 1.5 (DVDD>2.8V)	-	DVDD (DVDD<=2.8) 3.1 (DVDD>=2.8)	V
Low level input voltage	Vil	-0.3	-	0.3*DVDD[2]	V
High level output voltage (Ioh=2mA)	Voh	0.7*DVDD	-		V
Low level output voltage (Iol=2mA)	Vol	-	-	0.3	V
Input leakage current	Iil	-	-	±1	uA
Output leakage current	Iol	-	-	±1	uA
2.4V regulator	XV2.4	-	2.55	-	V
Mic_Bias 0, 1	Mic_Bias	-	1.9	-	V
Active mode power supply current[3]	I_{AVDD} I_{DVDD}	-	?	-	mA
Power-down power supply current	I_{AVDD} I_{DVDD}	-	?	-	uA
By-Pass power supply current	I_{AVDD} I_{DVDD}	-	?	-	mA
Suspend power supply current	I_{AVDD} I_{DVDD}	-	?	-	uA

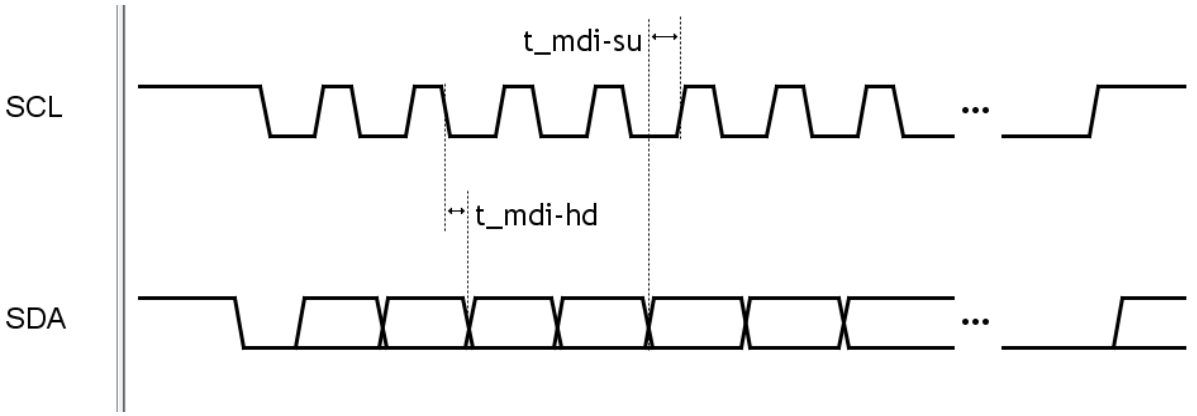
Notes：
1. Vih for Mode_Selector pin is recommended to be > 0.75*DVDD for corner case.
2. Vil for Mode_Selector pin is recommended to be < 0.23*DVDD for corner case.
3. Power supply test conditions: AV_{DD} = 2.8V, DVDD = 1.8V, clock= 26MHz, TA=+25°C, digital mic-in, digital mic-out, Mode_Select pin control mode. ENC enable.

8.4 I/O timing

8.4.1 I2C master interface



(a) I2C master data out



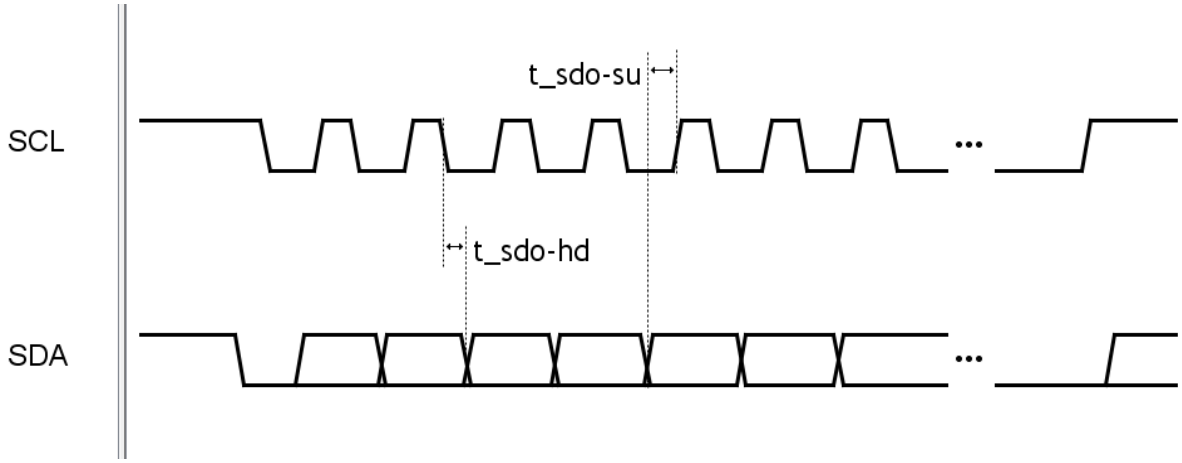
(b) I2C master data in

Fig. 8.1 I2C standard mode and fast mode timing (a) master data out (b) master data in.

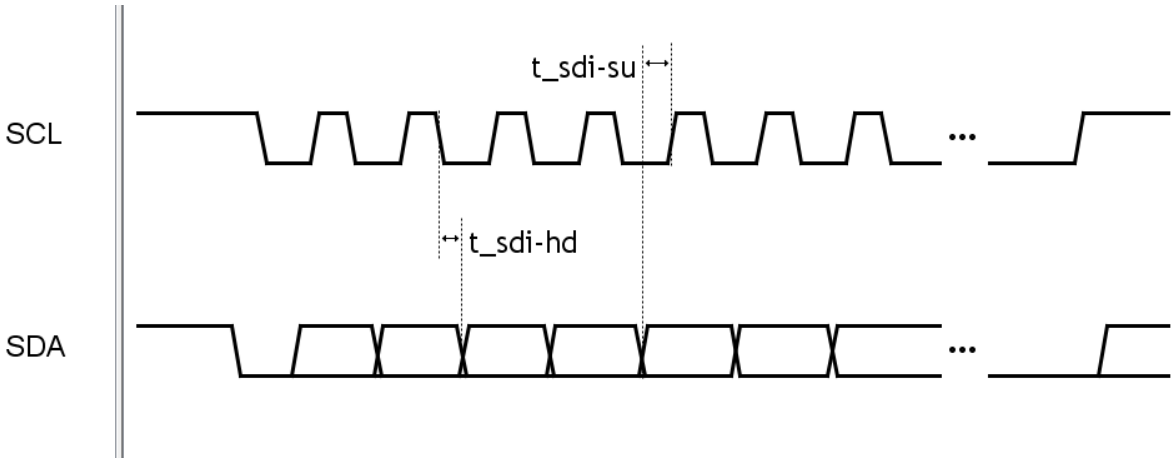
Parameter	Symbol	Standard mode	Fast mode	Unit
SCL clock frequency	f_scl	100	395.65	kHz
SCL clock period	t_scl	10	2.5275	us
Low period of SCL clock	t_low	4.68	1.325	us
High period of SCL clock	t_high	4.32	0.949	us
Hold time for START condition	t_s-hd	4.32	0.949	us
Setup time for STOP condition	t_p-su	4.32	0.949	us
Master DataOut setup time	t_mdo-su	4.32	0.949	us
Master DataOut hold time	t_mdo-hd	0.3758	0.3758	us
Master DataIn setup time	t_mdi-su	0.5	0.125	us
Master DataIn hold time	t_mdi-hd	0.04	0.04	us

Note **s**：Based on HCLK =45.5MHz

8.4.2 I2C slave interface



(a) I2C slave data out



(b) I2C slave data in

Fig. 8.2 I2C slave standard mode and fast mode timing (a) slave data out (b) slave data in.

Parameter	Symbol	Standard mode	Fast mode	Unit
Slave DataOut setup time	t_sdo-su	5.328	1.287	us
Slave DataOut hold time	t_sdo-hd	0.04	0.04	us
Slave DataIn setup time	t_sdi-su	0.5	0.125	us
Slave DataIn hold time	t_sdi-hd	0.004	0.004	us

Note：Based on HCLK =45.5MHz

8.4.3 I2S slave interface

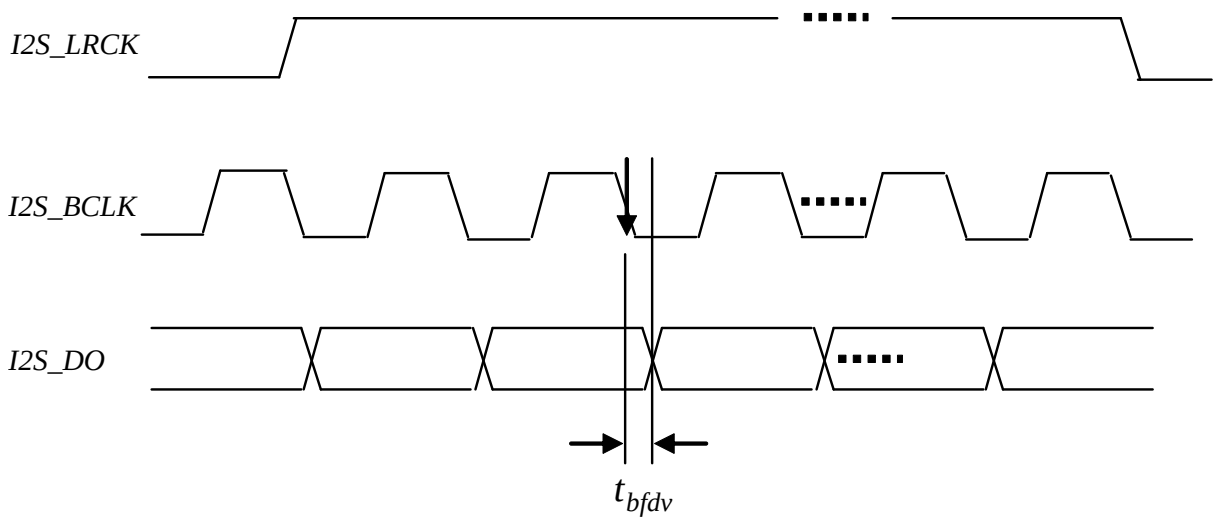


Fig. 8.2 I2S slave interface timing

Parameter	Symbol	Min	Max	Unit
I2S_BCLK falling edge to I2S_DO data valid	t_{bfdv}	12	15	*nS*

8.4.4 UART baud rate tolerance

The tolerance of the various UART baud rate is listed in the following table.

Baud Rate	Tolerance Minimum	Tolerance Maximum	Unit
9600	9280	9673	bps
19200	18575	19352	bps
57600	55798	58367	bps
115200	111597	116666	bps

8.4.5 digital microphone output

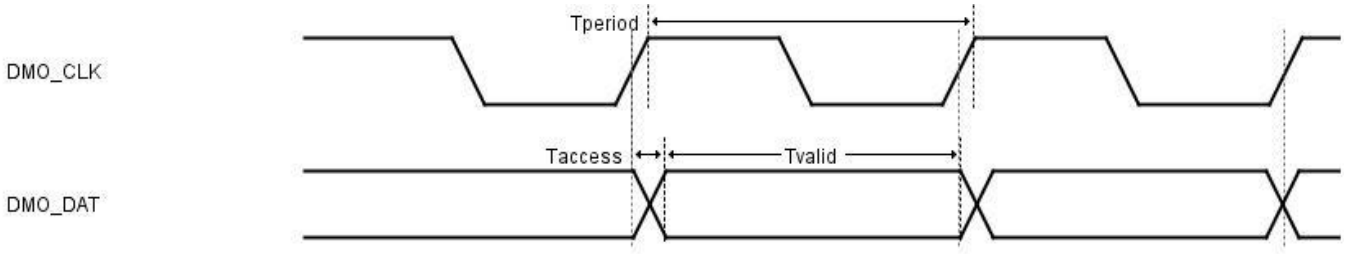


Fig. 8.3 Timing Diagram of Digital Microphone output.

Parameter	Symbol	Value	Unit
DMO input clock period	Tperiod	483.5*	ns
Data access times after clock rising edge	Taccess	11	ns
Data valid time	Tvalid	472.5	ns

*The DMO input clock is expected to be around 2.068 MHz. When the DMO input clock is 2.068 MHz (483.5 ns), the sampling rate is 16.157 kHz (2.068 MHz / 128).

8.4.6 digital microphone input

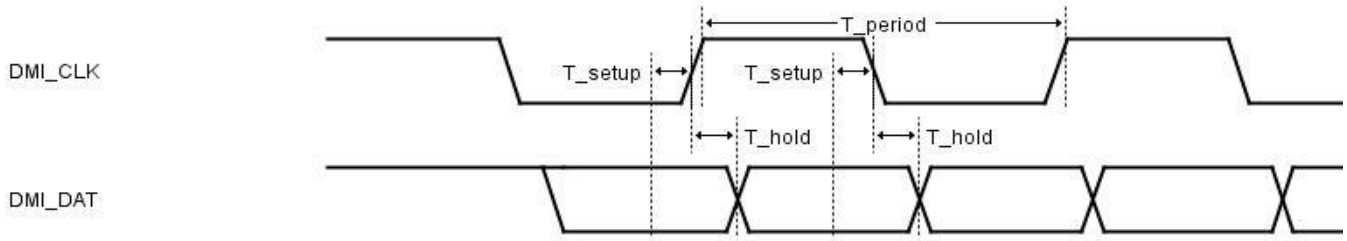


Fig. 8.4 Timing diagram of digital microphone input.

DMI Clock Select (dmi_clk_sel[1:0])	DMI Clock Source	DMI Output Clock Period (T_period)	DMI Input Data Setup Time (T_setup)	DMI Input Data Hold Time (T_hold)
00/11	Internal clock generator	483.5 ns	7ns	7ns
01	DMO clock input	The same as DMO clock input	7ns	7ns
10	BCLK I2S input	The same as I2S BCLK input	7ns	7ns

8.5 Analog performance

Test Conditions: AVDD = 2.8V, DVDD (V_{DD})= 1.8V DGND =0V, Fs= 16kHz, PGA Gain= 0dB, TA=+25°C, output loading=10K ohms, mic-in coupling capacitor= 220nF, w/ 8kHz Filter

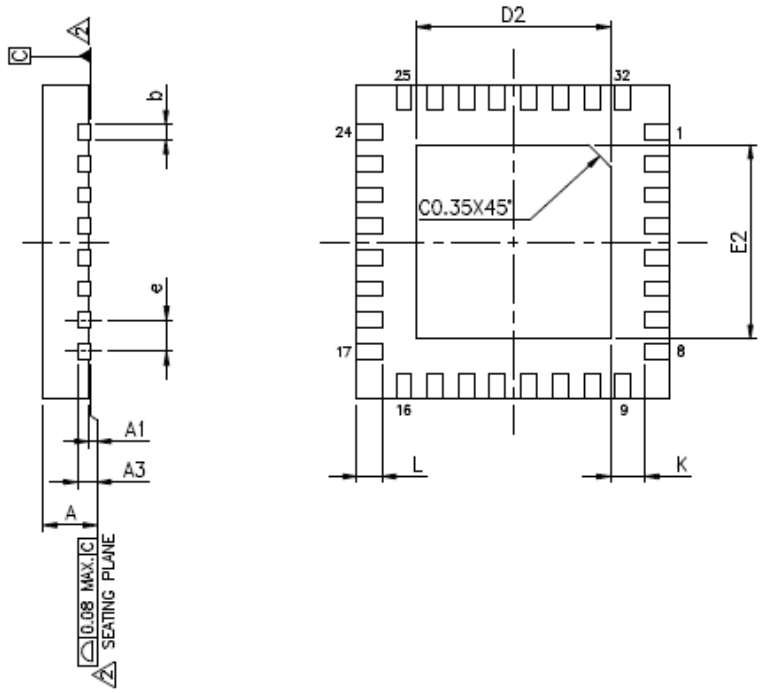
Item	Min.	Typ.	Max.	Unit
ADC Performance				
Resolution	-	16	-	bit
Sample rate	-	16K	-	Hz
THD + N (@1kHz)	-	-60	-	dBFS
SNR (@1kHz)	85	90	-	dBFS
Dynamic range (@1kHz)	85	90	-	dBFS
Frequency response (-3dB/-9dB)	60	-	6.8K	Hz
Passband ripple	-	±0.25	-	dBFS
Single-ended full-scale input voltage	-	1.41[1]	-	Vp-p
differential full-scale input voltage	-	2.82[1]	-	Vp-p
Power supply rejection ratio (217Hz)		85		dB
Microphone/Aux Input				
Mic-in PGA gain range	0	+20 (default)	+31	dB
Aux-in PGA gain range	-12	+8 (default)	+19	dB
ADC PGA gain step	-	1	-	dB/Step
Mic input impedance	-	15K	-	Ω
Aux input impedance		60K		Ω
Microphone bias voltage	-	1.9	-	V
DAC Performance (10K Ohm Line Loading)				
Resolution	-	16	-	Bits
Sample rate		16K		Hz
THD + N (@1kHz)	-	-67.5	-	dBFS
SNR (@1kHz)	-	90	-	dBFS
Dynamic range (@1kHz)	-	85.5	-	dBFS
Frequency response (-3dB/-3dB)	20	-	6.8K	Hz
Passband ripple	-	+-0.1	-	dBFS
Single-ended full-scale output voltage	-	1.41	-	Vp-p
Differential full-scale output voltage	-	2.82	-	Vp-p
Power supply rejection ratio (217Hz)		80		dB
DAC/Analog Output Gain				
DAC PGA gain range	-31	-17 (default)	0	dB
DAC PGA gain step	-	1	-	dB/Step

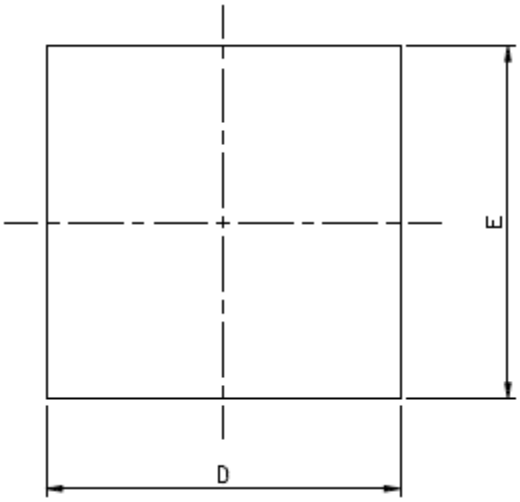
Note：Although the full-scale input voltage can be as high as 1.55Vp-p, the recommended maximum input voltage is below 1.41Vp-p (500mVrms) for single-ended input, 2.82Vp-p (1.0Vrms) for differential input to reserve the best signal linearity.

9 Package dimensions

9.1 CM7001 package dimensions

9.2 CM7001N package dimensions





SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.50 BSC.	
L	0.35	0.40	0.45
K	0.20	—	—

UNIT : mm

	D2			E2		
EXPOSED PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
3.2X3.2	3.10	3.20	3.30	3.10	3.20	3.30

UNIT : mm

NOTES :

1. JEDEC OUTLINE : N/A.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

—End of Datasheet—

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