SiI9293 MHL/HDMI Receiver

Data Sheet

Document # SiI-DS-1107-A

March 2013

Copyright Notice

Patents

The subject matter described herein may contain one or more inventions claimed in patents or patents pending owned by Silicon Image, Inc. or its affiliates.

Trademark Acknowledgment

Silicon Image®, the Silicon Image logo, Instaport®, the Instaport logo, InstaPrevue®, Simplay®, Simplay HD®, and UltraGig™ are trademarks or registered trademarks of Silicon Image, Inc. in the United States or other countries. HDMI® and the HDMI logo with High-Definition Multimedia Interface are trademarks or registered trademarks of, and are used under license from, HDMI Licensing, LLC. in the United States or other countries. MHL® and the MHL logo are trademarks or registered trademarks of, and are used under license from, MHL, LLC. in the United States or other countries. WirelessHD®, the WirelessHD logo, WiHD® and the WiHD logo are trademarks, registered trademarks or service marks of SiBeam, Inc. in the United States or other countries.

HDMI Licensing, LLC; MHL, LLC; Simplay Labs, LLC; and SiBeam, Inc. are wholly owned subsidiaries of Silicon Image, Inc.

All other trademarks and registered trademarks are the property of their respective owners in the United States or other countries. The absence of a trademark symbol does not constitute a waiver of Silicon Image's trademarks or other intellectual property rights with regard to a product name, logo or slogan.

Export Controlled Document

This document contains information subject to the Export Administration Regulations (EAR) and has a classification of EAR99 or is controlled for Anti-Terrorism (AT) purposes. Transfer of this information by any means to an EAR Country Group E:1 or foreign national thereof (whether in the U.S. or abroad) may require an export license or other approval from the U.S. Department of Commerce. For more information, contact the Silicon Image Director of Global Trade Compliance.

Further Information

To request other materials, documentation, and information, contact your local Silicon Image, Inc. sales office or visit the Silicon Image, Inc. web site at www.siliconimage.com.

Revision History

Revision	Date	Comment
A	03/2013	First production release.

Table of Contents

List of Figures

List of Tables

General Description

The Silicon Image SiI9293 device is the first combined Mobile High-definition Link (MHL™) 2 and standard High Definition Multimedia Interface (HDMI™) 1.4 Receiver. The receiver features MHL input up to 1080p60 and 3D 1080p30 Frame Sequential, and facilitates DTVs to support MHL and HDMI together.

Furthermore, efficient color space conversion converts RGB or YCbCr video data input to either standard-definition or high-definition RGB or YCbCr formats.

The SiI9293 receiver is preprogramed with High-bandwidth Digital Content Protection (HDCP) Keys and contains an integrated HDCP decryption engine for receiving protected audio and video content.

The MHL/HDMI core of the SiI9293 device uses the latest generation Transition Minimized Differential Signaling (TMDS™) core technology.

MHL/HDMI Inputs

- MHL, HDMI and Digital Visual Interface (DVI) compatible input port
- The TMDS™ core runs up to 3.0Gbps
- Supports up to1080p60 and 3D 1080p30 in Packed Pixel mode for MHL input
- Top-bottom, Left-right, and Frame Sequential MHL 3D video mode support
- Supports HDMI input formats up to 1080p60 and 3D 1080p30 Frame Packing
- HDMI input support up to UXGA
- Dynamic cable equalization automatically detects the equalization required for the incoming signal
- Low power 1.0 V core

Digital Video Output

- Flexible support for many different standard and high-definition video formats (16/20/24-bit YCbCr 4:2:2, 24-bit RGB/YCbCr 4:4:4)
- 12-bit Digital Multimedia Output (DMO) RGB/YCbCr 4:4:4 (clocked with rising and falling edges) and 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- xvYCC color space to extended RGB support

Digital Audio Interface

- One I^2S output lane supports two audio channels
- Time-Diversion Multiplexing (TDM) audio interface supports up to eight audio channels
- S/PDIF output supports multichannel Dolby Digital, DTS, MPEG2 Audio, and two channel PCM (32 kHz – 192 kHz f_S sample rate)
- Intelligent audio mute capability avoids pops and noise with automatic soft mute and unmute

Control

- Consumer Electronics Control (CEC) interface incorporates an HDMI CEC I/O and integrated CEC Programming Interface (CPI)
- A single-wire control bus supports all sideband signaling for Display Data Channel (DDC), CEC, and Hot Plug Detect (HPD) with MHL input

Packaging

- 72-pin QFN package, 10mm x 10mm body size
- Extended temperature range (–20 ℃ to +85 ℃)

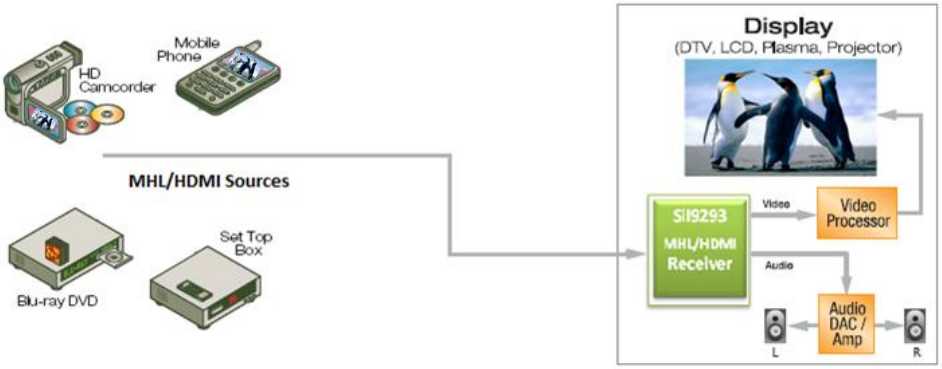


Figure 1. Typical Application

Pin Mapping

Figure 2 shows the pin diagram for the SiI9293 receiver. See the Pin Descriptions section beginning on page 24 for a detailed description of the pin functions.

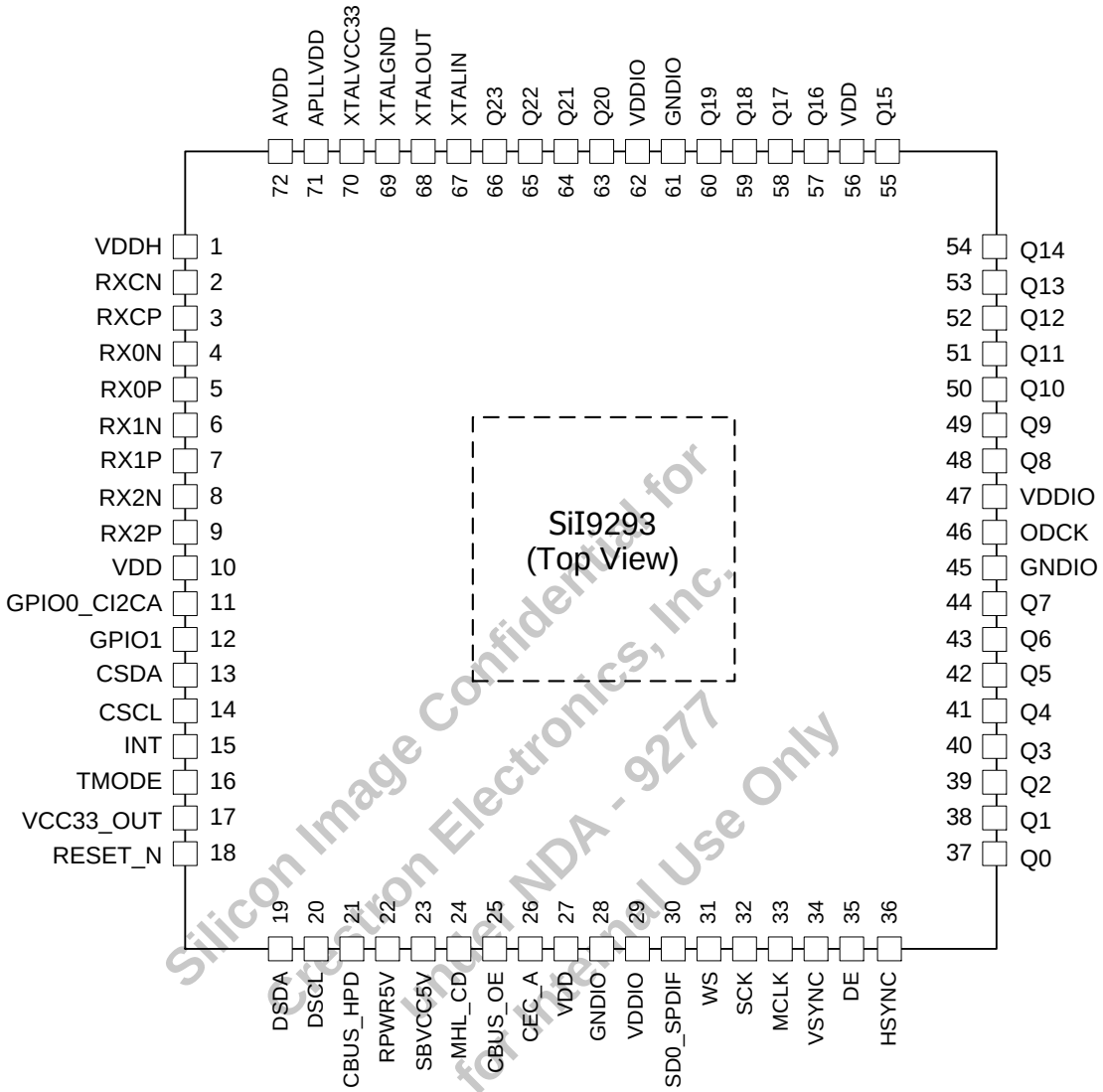


Figure 2. Pin Mapping

Functional Description

The SiI9293 receiver offers one input port that can both receive the MHL signals and HDMI signals. The SiI9293 device receives MHL/HDMI signals, and decodes them into RGB or YCbCr video output with digital parallel interface and digital audio output.

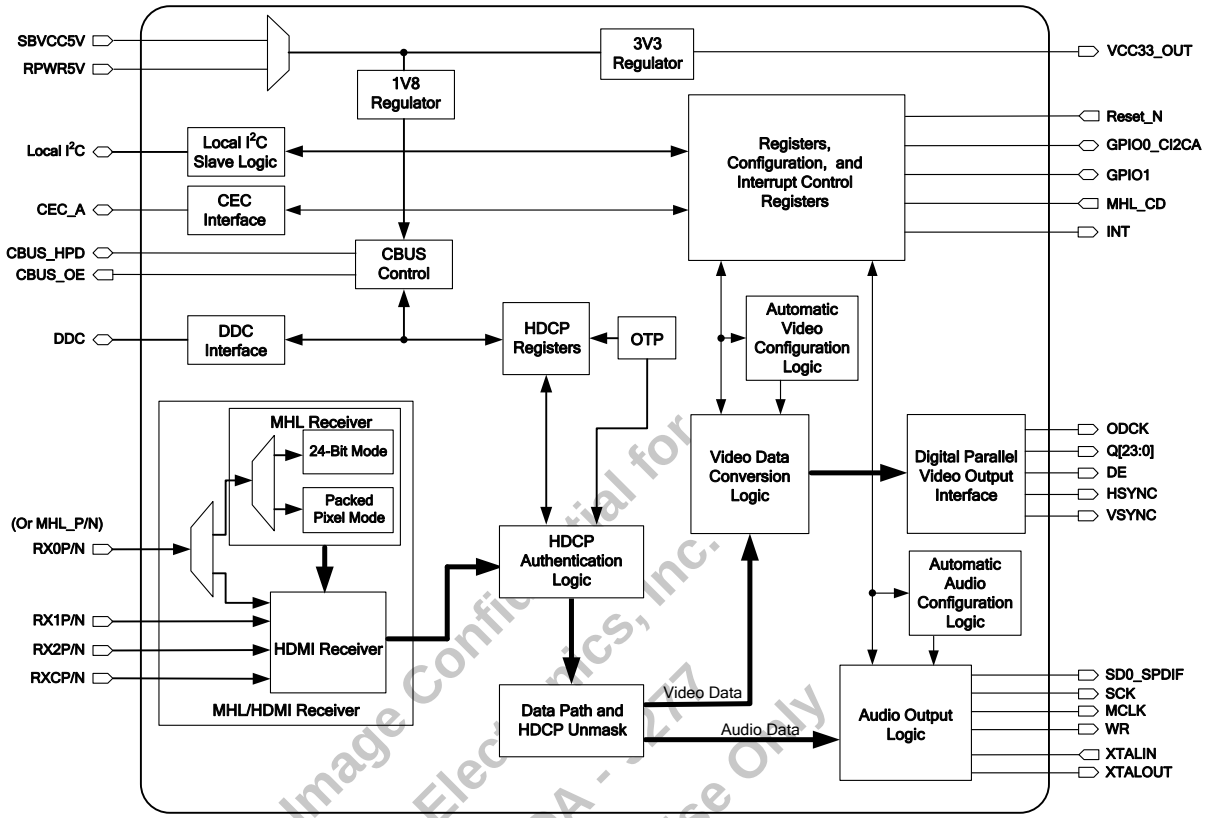


Figure 3. Functional Block Diagram

MHL/HDMI Receiver Block

The MHL/HDMI receiver block consists of a standard HDMI three-channel plus clock TMDS interface in addition to the MHL interface. The interface is selected depending on which mode the device is in. For example, when the device is configured as an MHL Receiver device, the input is configured for MHL input only. In the MHL mode, the source video and audio is formatted as the MHL protocol. The MHL receiver circuitry recovers the data and passes it on for conversion back to the three-channel HDMI signal.

The SiI9293 receiver supports two types of pixel encoding for the MHL mode, which are 24-bit mode and Packed Pixel mode. Refer to MHL 24-bit Mode and MHL Packed Pixel Mode sections on page 28 for more details.

CBUS Control Block

The CBUS signal handles the MHL Control Bus Interface. The MHL transmitter and receiver follow a specific communication and arbitration protocol to exchange EDID, Control, and HDCP information that would normally pass over the DDC clock and data wires. In addition, device remote control commands and hot plug status are also exchanged. All of the communication is managed transparently, so the source and bridge logic operate as if they had discrete DDC, control, and HPD signals.

HDCP Register Block

The HDCP Register Block controls the necessary logic to decrypt the incoming audio and video data. The decryption process is controlled entirely by the host-side microcontroller using a set sequence of register reads and writes through the DDC channel. The decryption process uses preprogrammed HDCP keys and a Key Selection Vector (KSV) stored in the on-chip OTP ROM.

OTP ROM Block

The One-Time Programmable (OTP) ROM Block is programmed at the factory and contains the preprogrammed HDCP keys. System manufacturers do not need to purchase key sets from Digital Content Protection, LLC. Silicon Image handles all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security, as the keys cannot be read out of the device after they are programmed.

HDCP Authentication Logic Block

The HDCP Authentication Block receiver handles the task of establishing a secure link for receiving protected content from upstream device. This process involves exchanging security information with the source over the CBUS, authenticating the source by computing a verification value that is, then compared to an equivalent value generated by the source, and enabling data decryption if both verification values match. A resulting calculated value is sent to HDMI Data Path and HDCP Unmask Block.

Data Path and HDCP Unmask Blocks

HDMI data from the MHL/HDMI Receiver are sent to and processed by the HDMI Receiver Data Path and HDCP Unmask Blocks. The appropriate decryption key is applied to the XOR mask in these blocks to descramble the video, audio, and auxiliary packets.

DDC Interface

The DDC interface provides a bidirectional I^2C port. In the MHL receiver mode, the DDC interface is part of the CBUS control block and works as an I^2C master. It is used to read EDID information from the external EEPROM. The DDC interface is encoded and decoded by the CBUS control block and sent over the CBUS interface to the MHL source device.

In the HDMI receiver mode, the HDMI source uses the DDC interface to read EDID information. And the DDC interface works as an I^2C slave and is used to exchange the HDCP information as well.

CEC Interface

The Consumer Electronics Control (CEC) Interface and CPI Register block provides CEC-compliant signals between the CEC devices and a CEC master. This CEC controller has a high-level register interface accessible through the I^2C interface, which is used to send and receive CEC commands. The I^2C interface is compatible with the Silicon Image CEC Programming Interface (CPI). This controller makes CEC control easy and straightforward, removing the burden of requiring the host processor performing these low-level transactions on the CEC bus.

Video Data Conversion Logic Block

The video data conversion logic block receives the output data from the Data Path and HDCP Unmask blocks. Figure 4 shows the processing stages for the video data. Each of the processing blocks can be bypassed by setting the appropriate register bits.

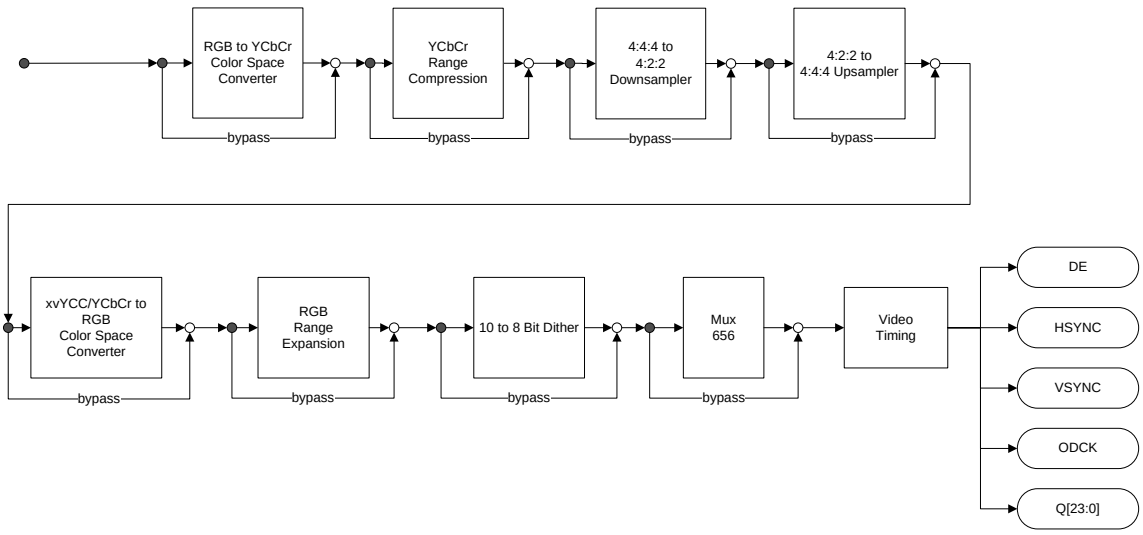


Figure 4. Default Video Processing Path

Color Space Converters

Color Space Converters (CSCs) are provided to convert RGB data to the Standard-definition (ITU.601) or High-definition (ITU.709) YCbCr formats, and vice-versa. To support the latest extended-gamut xvYCC displays, the SiI9293 device implements color space converter blocks to convert RGB data to the extended-gamut Standard-definition (ITU.601) or High-definition (ITU.709) xvYCC formats, and vice-versa. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

xvYCC Support

The SiI9293 receiver adds support for the extended gamut xvYCC color space only in the HDMI mode. This extended format has roughly 1.8 times more colors than the RGB color space. The use of the xvYCC color space is made possible because of the availability of LED and laser-based light sources for the next generation displays. This format also makes use of the full range of values (1 to 254) in an 8-bit space instead of 16 to 235 in the RGB format.

YCbCr Range Compression

When enabled by itself, the Range Compression Block compresses 0 – 255 full-range data into 16 – 235 limited-range data for each video channel, and compresses to 16 – 240 for the Cb and Cr channels. The color range scaling is linear.

4:4:4 to 4:2:2 Downsampler

Downsampling reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

4:2:2 to 4:4:4 Upsampler

Chrominance upsampling and downsampling increase or decrease the number of chrominance samples in each line of the video. Upsampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

RGB Range Expansion

The SiI9293 device can scale the input color from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16–235 limited-range data into 0 – 255 for each video channel. When the range expansion and the xvYCbCr/YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16 – 240.

10 to 8 Bit Dither

The 10 to 8 Bit Dither block dithers internally processed 10-bit data to 8-bit data for output.

Mux 656

The Mux 656 block multiplexes the video data into YC Mux (ITU.656) format.

Video Timing

The video timing block is used to control the timing of the digital parallel video output automatically according to the output format setting, such as controlling the output frequency of the ODCK, and disabling the HSYNC, VSYNC and DE signals output when the output format is set as embedded syncs.

Digital Parallel Video Output Interface

The SiI9293 receiver outputs the uncompressed digital video with a data width of 8 to 24 bits from the digital parallel video output interface. The data path has three 8-bit data channels, which can be configured in many different video formats. The supported typical 2D formats are listed in Table 1 below. Refer to 3D Video Formats on page 28 for the details of the supported 3D formats.

Table 1. Typical Digital Video Output 2D Formats

Color Space	Video Format	Bus Width	HSYNC/ VSYNC	Output Clock (MHz)								Notes
				480i/576i[2, 3]	480p	XGA	720p	1080i	SXGA	1080p	UXGA	
RGB	4:4:4	24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12	Separate	27	27	65	74.25	74.25	—	—	—	4
YCbCr	4:4:4	24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12	Separate	27	27	65	74.25	74.25	—	—	—	4
	4:2:2	16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	—	—
		16/20/24	Embedded	27	27	—	74.25	74.25	—	148.5	—	1
		8/10/12	Separate	27	54	—	148.5	148.5	—	—	—	—
		8/10/12	Embedded	27	54	—	148.5	148.5	—	—	—	1

Notes:

1. Embedded syncs use SAV/EAV coding.
2. 480i and 576i modes can output a 13.25 MHz clock using the internal clock divider.
3. Output clock frequency depends on programming of internal registers.
4. Output clock supports 12-bit mode by using dual edges.

Automatic Video Configuration Logic Block

The SiI9293 receiver Automatic Video Configuration (AVC) Logic simplifies the firmware's task of updating the video data conversion path whenever the incoming video changes format. When the AVC logic is enabled, bits of the incoming MHL/HDMI Auxiliary Video Information (AVI) InfoFrame and the configured output format are used to program the registers in the video path.

The AVC logic assumes that the AVI information is accurate. If the AVI information is not available, the SiI9293 receiver must choose the video path based on measurement of the incoming resolution.

The digital video output bus can be automatically configured to many different formats by programming the Auto Output Format Register.

Refer to the SiI9293 MHL/HDMI Receiver Programmer's Reference for details about how to set registers for automatic video configuration.

Audio Output Logic Block

The SiI9293 device supports S/PDIF, two channels I^2S, and up to eight channels TDM audio interface as audio output. The pins for each format are shared, thus only one audio interface is available at a time.

More information about audio support can be found in the Audio Output Interface section on page 29.

Automatic Audio Configuration Logic Block

The SiI9293 receiver Automatic Audio Configuration (AAC) Logic can control the audio output based on the current states of FIFO, Video, ECC, ACR, PLL, and InfoFrame. Audio output is enabled only when all necessary conditions are met. If any critical condition is missing, then the audio output is disabled automatically.

The AAC logic can trigger audio soft mute automatically, when there is an interruption to the MHL/HDMI audio stream (or an error). This feature is useful to prevent any audio pop from being sent to the I^2S, TDM or S/PDIF outputs.

Refer to the SiI9293 MHL/HDMI Receiver Programmer's Reference for details about how to set registers for automatic audio configuration.

Registers, Configuration, and Interrupt Logic Block

The registers, configuration, and interrupt logic block incorporates all the registers required for configuring and managing the features of the SiI9293 receiver. These registers are accessible from Local I^2C port. I^2C addresses of the device can be altered with the level of the CI2CA signal, as described in the Device Address Configuration Using CI2CA section on page 31.

The interrupt control logic generates or masks the INT signal, which can be used to interrupt the host processor on exceptional conditions. INT signaling defaults to active LOW (open drain) to allow sharing with other active LOW interrupt sources. However, it can be configured to active HIGH or push-pull.

Refer to the associated Programmer's Reference for more details about the registers and configuration.

Local I^2C Slave Logic Block

The local I^2C slave bus provides a communication interface from the host to the SiI9293 device. The controller I^2C interface on the SiI9293 receiver (signals CSCL and CSDA) is a salve interface capable of running up to 400 kHz (see parametric limitation above 100 kHz in Table 17 on page 16).

On-chip Regulator

The SiI9293 receiver contains two regulators (1.8 V and 3.3 V regulators) powered from the 5 V (RPWR5V or SBVCC5V) input. The on-chip regulators provide a low-cost system implementation.

1.8 V Regulator

The SiI9293 receiver internal 1.8 V Regulator provides 1.8 V for the internal CBUS only. This regulator is enabled automatically.

3.3 V Regulator

The internal 3.3 V regulator is an optional regulator that provides 3.3 V. The maximum output current of this regulator is 30 mA. The output pin of this regulator VCC33_OUT requires a 10 µF capacitor to ground.

Electrical Specifications

Table 2. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
SBVCC5V	Primary On-chip Regulator Supply Voltage	−0.3	—	5.7	V	1, 2, 3
RPWR5V	Supply Voltage	−0.3	—	5.7	V	1,2,3
VDD	Digital Core Supply Voltage	−0.3	—	1.25	V	1, 2
AVDD	Analog Core Supply Voltage	−0.3	—	1.25	V	1, 2
APLLVDD	Analog PLL Supply Voltage	−0.3	—	1.25	V	1, 2
VDDIO	Digital I/O Power Voltage	−0.3	—	4.0	V	1, 2
VDDH	TMDS I/O Supply Voltage	−0.3	—	4.0	V	1, 2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	−0.3	—	4.0	V	1, 2
V_I	Input Voltage	−0.3	—	VDDIO + 0.3	V	1, 2
V_O	Output Voltage	−0.3	—	VDDIO + 0.3	V	1, 2
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	−65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.

Table 3. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Note
Latch up	ESD Latch up	±200	—	—	mA	1, 2
HBM	Human Body Model	±4	—	—	kV	3
MM	Machine Model	±200	—	—	V	4
CDM	Charged Device Model	±1	—	—	kV	5
V_{ESD}	ESD voltage per IEC 61000-4-2 (Contact)	±8	—	—	kV	6
	ESD voltage per IEC 61000-4-2 (Air)	±8	—	—	kV	6

Notes:
1. At 70 ℃.
2. JESD78B standard.
3. JESD22-A114 standard.
4. JESD22-A115 standard.
5. JESD22-C101 standard.
6. System level tests at HDMI connectors.

Normal Operating Conditions

Table 4. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
SBVCC5V	Primary On-chip Regulator Supply Voltage	4.3	5.0	5.5	V	—
RPWR5V	Supply Voltage	4.3	5.0	5.5	V	—
VDD	Digital Core Supply Voltage	0.95	1.0	1.05	V	—
AVDD	Analog Core Supply Voltage	0.95	1.0	1.05	V	—
APLLVDD	Analog PLL Supply Voltage	0.95	1.0	1.05	V	—
VDDIO	Digital I/O Power Voltage	3.14	3.3	3.46	V	—
VDDH	TMDS I/O Supply Voltage	3.14	3.3	3.46	V	—
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	3.14	3.3	3.46	V	—
V_{DD33N}	3.3 V Supply Voltage Noise	—	—	100	mV_{P-P}	1
T_A	Ambient Temperature (with power applied)	–20	+25	+85	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	28	°C/W	3, 4
Θ_{jc}	Junction to Case Resistance (Theta JC)	—	—	14.4	°C/W	3, 4

Notes:

1. The supply voltage noise is measured at test point VDDTP, as shown in Figure 5 on page 10. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VDD pins as well.
2. The MHL VBUS voltage requirements may be more stringent than the 5 V power supply requirements for the receiver itself.
3. Airflow at 0 m/s.
4. The thermal resistance figures are based on a 4-layer PCB.

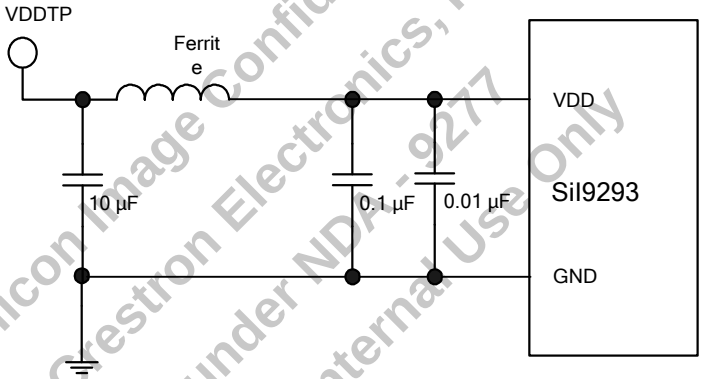


Figure 5. Test Point VDDTP for VDD Noise Tolerance Specification

DC Specifications

Table 5. Digital I/O Specifications

Symbol	Parameter	Pin Type[1]	Conditions	Min	Typ	Max	Units	Note
V_{IH}	HIGH Level Input Voltage	LVTTL	—	2.0	—	—	V	2
V_{IL}	LOW Level Input Voltage	LVTTL	—	—	—	0.8	V	2
$V_{TH+RESET\_N}$	LOW to HIGH threshold RESET_N pin	Schmitt	—	2.0	—	—	V	—
$V_{TH-RESET\_N}$	HIGH to LOW threshold RESET_N pin	Schmitt	—	—	—	0.8	V	—
V_{TH+DDC}	LOW to HIGH Threshold, DDC Bus	Schmitt	—	3.0	—	—	V	3
V_{TH-DDC}	HIGH to LOW Threshold, DDC Bus	Schmitt	—	—	—	1.5	V	3
V_{TH+I2C}	LOW to HIGH Threshold, I^2C Bus	Schmitt	—	2.0	—	—	V	—
V_{TH-I2C}	HIGH to LOW Threshold, I^2C Bus	Schmitt	—	—	—	0.8	V	—
V_{TH+CEC_A}	LOW to HIGH threshold, CEC_A pin	Schmitt	—	2.0	—	—	V	—
V_{TH-CEC_A}	HIGH to LOW threshold, CEC_A pin	Schmitt	—	—	—	0.8	V	—
V_{OL_DDC}	LOW Level Output Voltage	Open Drain	I_{OL} = – 3 mA	—	—	0.4	V	3
V_{OL_I2C}	LOW Level Output Voltage	Open Drain	I_{OL} = – 3 mA	—	—	0.4	V	—
I_{IL}	Input Leakage Current	LVTTL	High Impedance	−10	—	10	µA	—
I_{OL}	Output Leakage Current	LVTTL	High Impedance	−10	—	10	µA	—
I_{OD8}	7.5 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4 V	7.5	—	—	mA	4
			V_{OUT} = 0.4 V	7.5	—	—	mA	4

Notes:
1. Refer to the Pin Descriptions section on page 24 for pin type designations for all package pins.
2. Applies to the GPIO0_CI2CA and GPIO1 signal pins.
3. Applies to the DDC interface.
4. Applies to the GPIO0_CI2CA, GPIO1, and INT signal pins.

Table 6. Digital CBUS DC Specifications

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Units	Note
V_{IH_CBUS}	LOW to HIGH threshold, CBUS pin	CBUS	—	1.0	—	—	V	—
V_{IL_CBUS}	HIGH to LOW threshold, CBUS pin	CBUS	—	—	—	0.6	V	—
V_{OH_CBUS}	Output HIGH Voltage, CBUS pin	CBUS	I_O = 100 µA	1.5	—	1.9	V	—
V_{OL_CBUS}	Output LOW Voltage, CBUS pin	CBUS	I_O = 100 µA	—	—	0.2	V	—
I_{OH_CBUS}	HIGH output drive current	CBUS	VOH = 1.5 V	2	—	—	mA	—
I_{OL_CBUS}	LOW output drive current	CBUS	VOL = 0.2 V	300	—	—	µA	—
I_{IL}/I_{IH}	Input Leakage Current	CBUS	High impedance	–1.0	—	1.0	µA	—
$Z_{CBUS\_SINK\_DISCOVER}$	Pull down resistance – discovery	CBUS	—	800	1000	1200	Ω	—
$Z_{CBUS\_SINK\_ON}$	Pull down resistance – ON	CBUS	—	90	100	110	kΩ	—

Table 7. DC Power Supply Specifications

Symbol	Parameter	Output Frequency	Typical[3]			Maximum[4]			Units	Note
			5 V	3.3 V[1]	1.0 V[2]	5.5 V	3.46 V[1]	1.05 V[2]		
I_{DDSB}	Standby current	—	6.3	4.0	32	7.7	5.8	70	mA	—
MHL Input										
I_{DDFP}	Full operation current	25 MHz	6.3	53	63	8.0	60	120	mA	5
		75 MHz	6.3	82	95	8.0	96	123	mA	6
		150 MHz	6.3	130	103	8.0	140	180	mA	7
HDMI Input										
I_{DDFP}	Full operation current	25 MHz	6.3	70	47	7.7	77	110	mA	5
		75 MHz	6.3	100	70	7.7	110	135	mA	6
		150 MHz	6.3	160	85	7.7	175	155	mA	7

Notes:

1. The power includes VDDIO, VDDH, and XTALVCC33. Power consumption of VDDH depends on the MHL and HDMI source devices.
2. The power includes VDD, AVDD, and APLLVDD.
3. Typical power specifications measured with supplies at typical normal operating conditions, default output swing control register setting, and a sweep video pattern along with 2-channel 48 kHz I^2S audio output.
4. Maximum power limits measured with all the power supplies at maximum normal operating conditions, maximum normal operating ambient temperature, default output swing control registers setting, and a sweep video pattern along with 2-channel 48 kHz I^2S audio output.
5. The input video format is 480p @ 60 fps.
6. The input video format is 720p @ 60 fps.
7. The input video format is 1080p @ 60 fps.

Table 8. TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Voltage	—	V_{TERM} – 400	—	V_{TERM} – 37.5	mV

Table 9. TMDS Input DC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	V_{TERM} – 1200	—	V_{TERM} – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min(720, 0.85 V_{IDF})	mV

AC Specification

Table 10. TMDS Input Timing AC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
$T_{INTRA-PAIR\_SKEW}$	Input Intrapair Skew	—	—	—	0.4	T_{BIT}	—
$T_{INTER-PAIR\_SKEW}$	Input Interpair Skew	—	—	—	$0.2T_{PIXEL}$ + 1.78	ns	—
F_{RXC}	Differential Input Clock Frequency	—	25	—	165	MHz	—
T_{RXC}	Differential Input Clock Period	—	6.06	—	40	ns	—
T_{IJIT}	Differential Input Clock Jitter Tolerance	165 MHz	—	—	0.3	T_{BIT}	—

Table 11. TMDS Input Timing AC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SKEW_DF}	Input Differential Intrapair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common-mode Intrapair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	75	MHz
T_{RXC}	Differential Input Clock Period	—	13.33	—	40	ns
T_{CLOCK_JIT}	Common-mode Clock Jitter Tolerance	≤ 2.25 Gbps	—	—	$0.3T_{BIT}$ + 266.7	ps
		> 2.25 Gbps	—	—	$0.9T_{BIT}$	
T_{DATA_JIT}	Differential Data Jitter Tolerance	≤ 2.25 Gbps	—	—	$0.4T_{BIT}$ + 88.88	ps
		> 2.25 Gbps	—	—	$0.6T_{BIT}$	

Video Output Timings

Table 12. Video Data Output AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	LOW-to-HIGH Rise Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 10	2
D_{HLT}	HIGH-to-LOW Fall Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 10	2
T_{CIP}	ODCK Cycle Time	C_L = 10 pF	6.06	—	40	ns	Figure 11	—
F_{CIP}	ODCK Frequency	C_L = 10 pF	25	—	165	MHz	—	5
T_{DUTY}	ODCK Duty Cycle	≤ 75 MHz	40%	—	60%	T_{CIP}	Figure 11	3,7
		> 75 MHz	30%	—	70%			
T_{CK2OUT}	ODCK-to-Output Delay	C_L = 10 pF	0.4	—	2.5	ns	Figure 11	—

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L=10 pF.
2. Rise time and fall time specifications apply to HSYNC, VSYNC, DE, ODCK and Q[23:0].
3. Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a component of output setup and hold times.
4. See Table 20 on page 23 for calculation of worst case output setup and hold times.
5. All output timings are defined at the maximum operating ODCK frequency, F_{CIP}, unless otherwise specified.
6. T_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
7. RGB/YCbCr Dual-edge mode supports up to 720p60.

Audio Output Timings

Table 13. I^2S Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{TR}	SCK Clock Period (TX)	C_L = 10 pF	1.00	—	—	T_{TR}	Figure 12	1
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR}$ – 5	—	—	ns		1
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR}$ – 5	—	—	ns		1
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{TR}		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5	—	+5	ns		2
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. Refer to Figure 12 on page 20. Meets timings in Philips I^2S Specification.
2. Applies also to SD-to-WS delay.

Table 14. TDM Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_TDM}	Sample Rate	2-8 Channel	32	—	192	kHz	—	2
T_{SCKCYC}	TDM SCK Cycle Time	C_L = 10 pF	—	1.0	—	UI	Figure 13	1
$T_{SCKDUTY}$	TDM SCK Duty Cycle	C_L = 10 pF	40	—	60	%UI		1
T_{TDMSU}	Setup Time, SCK to FS/SD	C_L = 10 pF	0.4UI – 3.5	—	—	ns		1
T_{TDMHD}	Hold Time, SCK to FS/SD	C_L = 10 pF	0.4UI – 3.5	—	—	ns		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–3.5	—	+3.5	ns		—
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. Proportional to unit time (UI), according to sample rate.
2. The video mode that is lower than 720p does not support multichannel 192 kHz sample rate.

Table 15. S/PDIF Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPCYC}	SPDIF Cycle Time	C_L = 10 pF	—	2.0	—	UI	Figure 14	1, 2
F_{SPDIF}	SPDIF Frequency	—	4	—	24	MHz		3
T_{SPDUTY}	SPDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI		2, 5
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20	—	250	ns	Figure 15	1, 2, 4
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4	—	50	MHz		1, 2, 4
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLK\ CYC}$		2, 4
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. SPDIF is not a true clock, but is generated from the internal 128 f_s clock, for f_s from 128 to 512 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its use as an S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1 UI.

Table 16. Audio Crystal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{XTAL}	External Crystal Freq	—	26	27	28.5	MHz	Figure 6	—

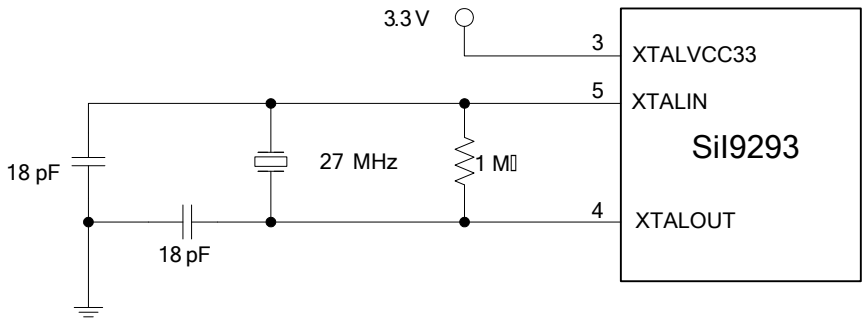


Figure 6. Audio Crystal Schematic

Miscellaneous Timings

Table 17. Miscellaneous Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid delay from SCL falling edge	C_L = 400 pF	—	—	700	ns	—	—
F_{DDC}	Speed on TMDS DDC Ports	C_L = 400 pF	—	—	100	kHz	—	3
F_{I2C}	Speed on Local I^2C Port	C_L = 400 pF	—	—	400	kHz	—	4
T_{RESET}	RESET_N Signal LOW Time for valid reset	—	2	—	—	ms	Figure 8	—
T_{RESET_VDD}	Time required for RESET_N high before VDD	50% RESET_N to 90% VDD	1	—	—	µs	Figure 9	5
$T_{SBVCC5RT}$	SBVCC5V Rise Time	10% – 90%	—	—	1	ms	—	—

Notes:

1. Guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
3. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I^2C standard mode timings.
4. Local I^2C port (CSCL/CSDA) meets standard mode I^2C timing requirements to 400 kHz.
5. This time is required due to internal Power-on Reset.

Interrupt Timings

Table 18. Interrupt Output Pin Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{FSC}	Link disabled (DE inactive) to SCDT LOW	—	—	0.15	40	ms	Figure 7	1, 2, 3, 8
T_{HSC}	Link enabled (DE active) to SCDT HIGH	—	—	—	4	DE	Figure 7	1, 2, 4, 8
T_{CICD}	RXC inactive to CKDT LOW	—	—	—	100	µs	Figure 7	1, 2, 8
T_{CACD}	RXC active to CKDT HIGH	—	—	—	10	µs	Figure 7	1, 2, 8
T_{INT}	Response Time for INT from Input Change	—	—	—	100	µs	—	1, 5, 8
T_{CIOD}	RXC inactive to ODCK inactive	—	—	—	100	ns	—	1, 8
T_{CAOD}	RXC active to ODCK active and stable	—	—	—	10	ms	—	1, 6, 8
T_{SRRF}	Delay from SCDT rising edge to Software Reset falling edge	—	—	—	100	ms	Figure 8	7

Notes:

1. Guaranteed by design.
2. SCDT and CKDT are register bits in this device.
3. SCDT changes to LOW after DE is HIGH for approximately 4096 pixel clock cycles, or after DE is LOW for approximately 1,000,000 clock cycles. At 27 MHz pixel clock, this delay for DE HIGH is approximately 150 µs, and the delay for DE LOW is approximately 40 ms.
4. SCDT changes to HIGH when clock is active (T_{CACD}) and at least 4 DE edges have been recognized. At 720p, the DE period is 22 µs, so SCDT responds approximately 50 µs after T_{CACD}.
5. The INT pin changes state after a change in input condition when the corresponding interrupt is enabled.
6. Output clock (ODCK) becomes active before it becomes stable. Use the SCDT signal as the indicator of stable video output timings, as this depends on decoding of DE signals with active RXC (see T_{FSC}).
7. Software Reset must be asserted and then de-asserted within the specified maximum time after rising edge of Sync Detect (SCDT). Access to both SWRST and SCDT can be limited by the speed of the I^2C connection.
8. SCDT is HIGH only when CKDT is also HIGH. When the receiver is in a powered-down mode, the INT output pin indicates the current state of SCDT. Thus, a power-down receiver signals a microcontroller connected to the INT pin whenever SCDT changes from LOW to HIGH or HIGH to LOW.

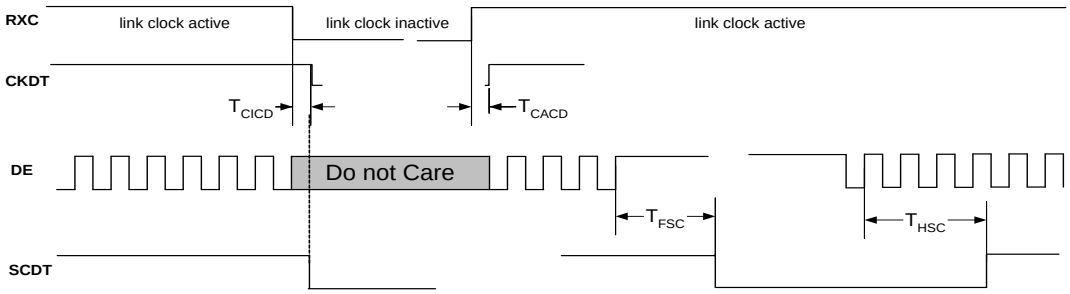


Figure 7. SCDT and CKDT Timing from DE or RXC Inactive/Active

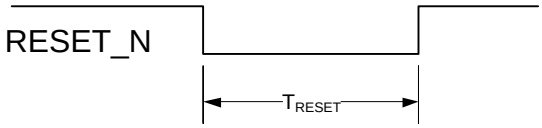
Notes:

1. The SCDT shown in Figure 7 is a register bit. SCDT remains HIGH if DE is stuck in LOW while RXC remains active, but SCDT changes to LOW if DE is stuck HIGH while RXC remains active.
2. The CKDT shown in Figure 7 is a register bit. CKDT changes to LOW whenever RXC stops, and changes to HIGH when RXC starts. SCDT changes to LOW when CKDT changes to LOW.
3. SCDT changes to LOW when CKDT changes to LOW. SCDT changes to HIGH at T_{HSC} after CKDT changes to HIGH.
4. The INT output pin changes state after the SCDT or CKDT register bit is set or cleared if those interrupts are enabled.

Refer to the SiI9293 MHL/HDMI Receiver Programmer's Reference for more details on controlling timing modes.

Timing Diagrams

Power sequencing is not required for SiI9293 device. However, to ensure a proper RESET the rules mentioned under the diagrams in Figure 8 and Figure 9 must be followed.



RESET_N must be pulled LOW for T_{RESET} before accessing registers. This is done by pulling RESET_N LOW from a HIGH state (shown above) for at least T_{RESET}.

Figure 8. RESET_N Minimum Timings

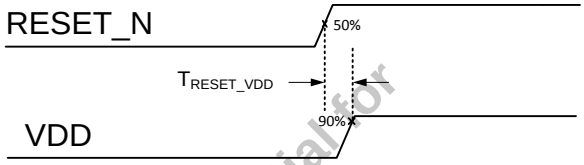


Figure 9. RESET_N to VDD Timing

Digital Video Output Timing Diagrams

Output Transition Times

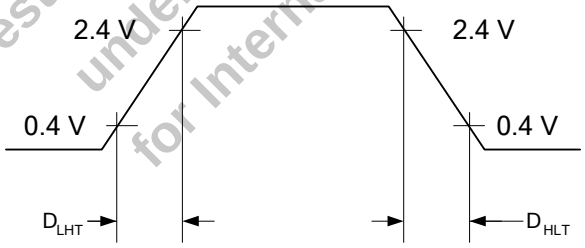


Figure 10. Video Digital Output Transition Times

Output Clock to Output Data Delay

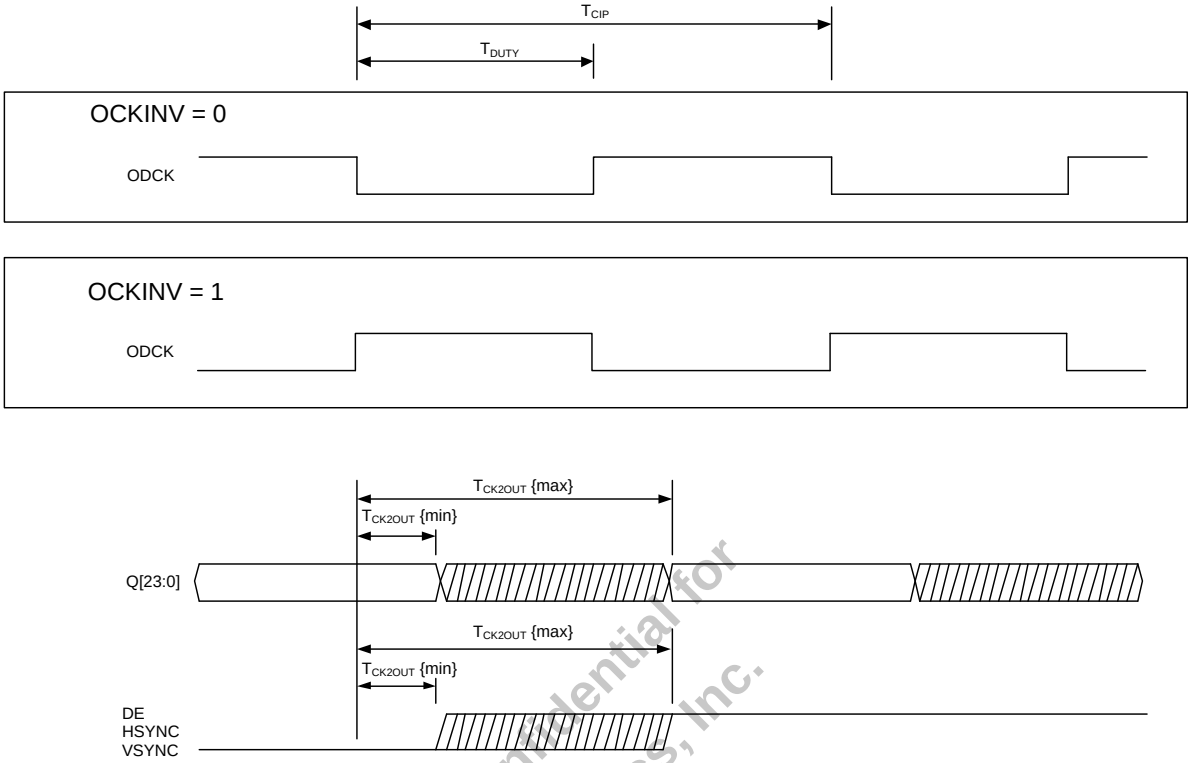


Figure 11. Receiver Clock-to-Output Delay and Duty Cycle Limits

Digital Audio Output Timings

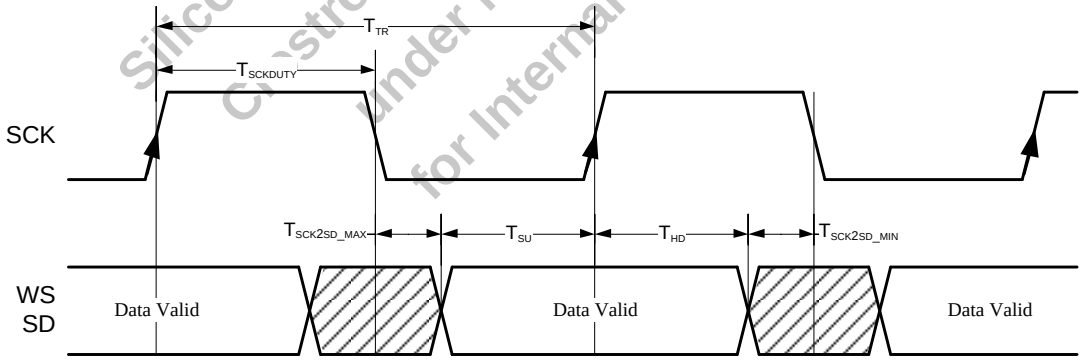


Figure 12. I²S Output Timings

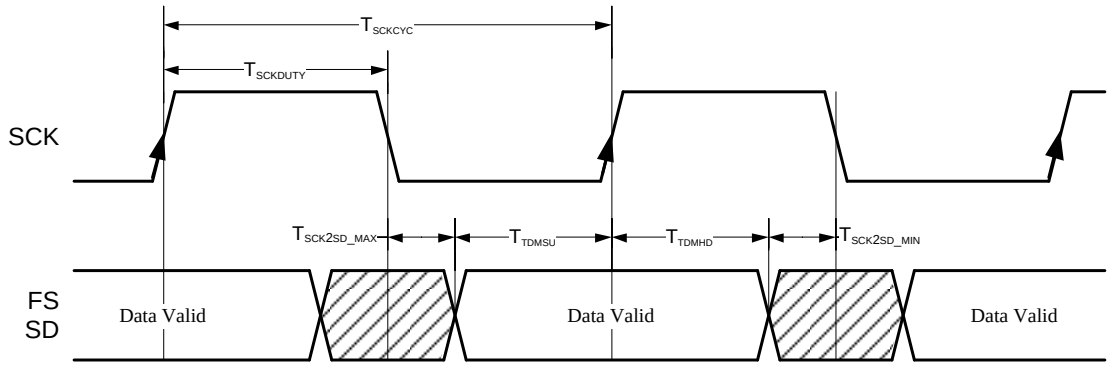


Figure 13. TDM Output Timings

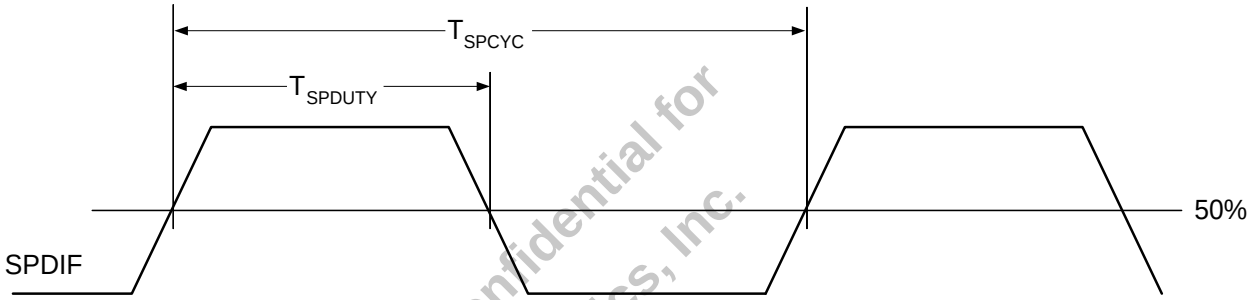


Figure 14. S/PDIF Output Timings

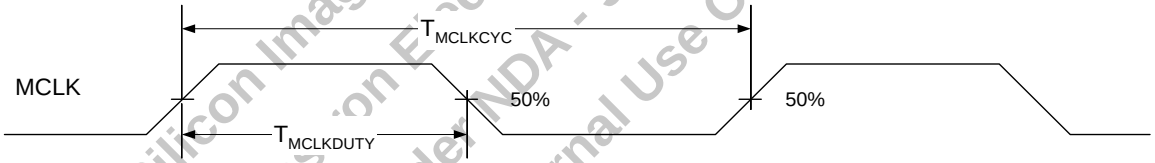


Figure 15. MCLK Timings

Calculating Setup and Hold Times for Video Bus

Normal Mode

Output data is clocked out on one rising (or falling) edge of ODCK, and then is captured downstream using the same polarity ODCK edge one clock period later. The setup time of data to ODCK and hold time of ODCK to data are therefore a function of the worst case ODCK to output delay, as shown in Figure 16. The active rising ODCK edge is shown with an arrowhead. For OCKINV=1, reverse the logic.

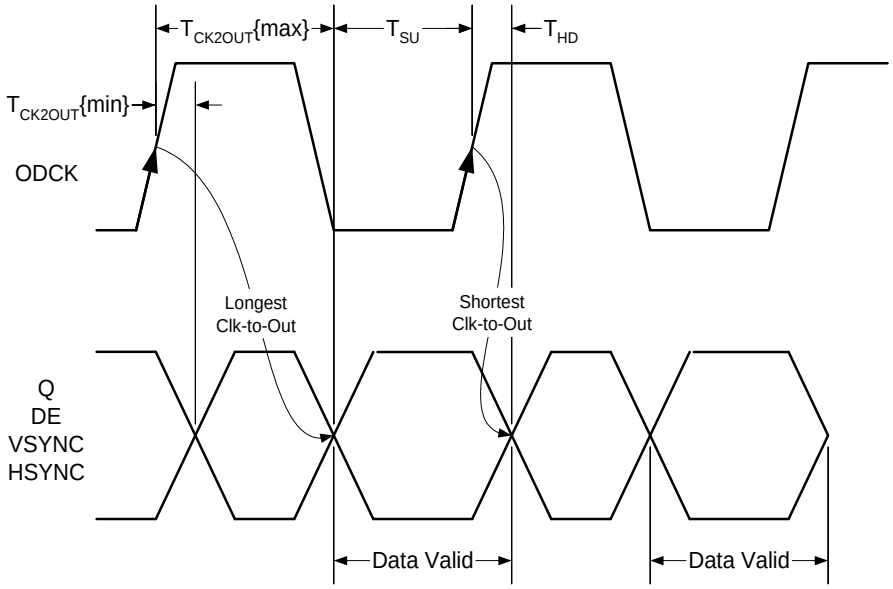


Figure 16. 24-Bit Mode Receiver Output Setup and Hold Times

Table 19 shows minimum calculated setup and hold times for commonly used ODCK frequencies. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10pF. These are approximations. Hold time is not related to ODCK frequency.

Table 19. Calculation of 24-bit Output Setup and Hold Times

	Symbol	Parameter	F_{ODCK}	T_{ODCK}	Min
24-bit Mode	T_{SU}	Setup Time to ODCK = $T_{ODCK} - T_{CK2OUT}$ {max}	27 MHz	37.0 ns	34.5 ns
			74.25 MHz	13.5 ns	11 ns
			148.5 MHz	6.7 ns	4.2 ns
	T_{HD}	Hold Time from ODCK = T_{CK2OUT} {min}	27 MHz	37.0 ns	0.4 ns
			74.25 MHz	13.5 ns	0.4 ns
			148.5 MHz	6.7 ns	0.4 ns

Dual-edge Mode

Output data is clocked out on each edge of ODCK (both rising and falling), and is then captured downstream using the opposite ODCK edge. This is shown in Figure 17. The setup time of data to ODCK is a function of the shortest duty cycle and the longest ODCK to output delay. The hold time does not depend on duty cycle (since every edge is used), and is a function only of the shortest ODCK to output delay.

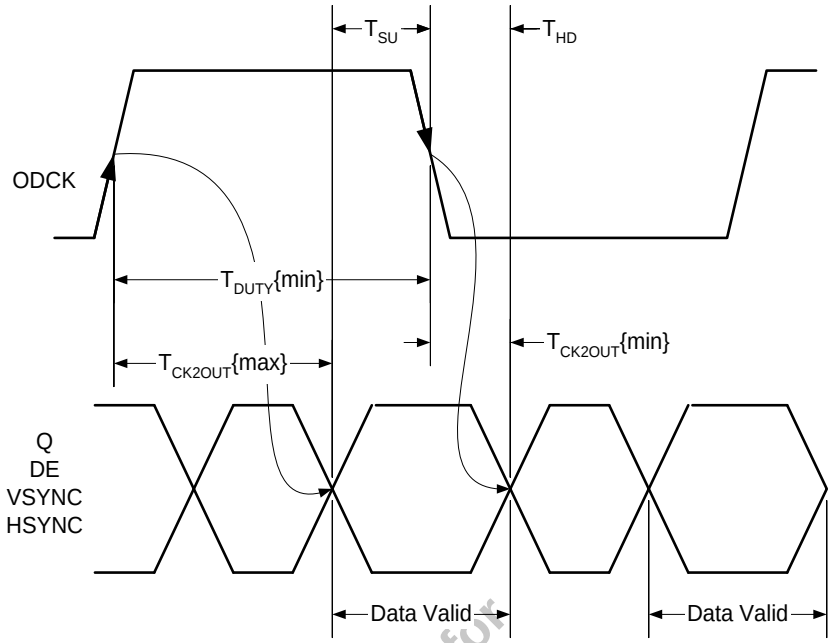


Figure 17. 12-bit Mode Receiver Output Setup and Hold Times

Table 20 shows minimum calculated setup and hold times for commonly used ODCK frequencies, up to the maximum allowed for 12/15/18-bit mode. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 20. Calculation of 12-bit Output Setup and Hold Times

	Symbol	Parameter	T_{ODCK}		Min
12-bit Mode	T_{SU}	Setup Time to ODCK = T_{ODCK} • T_{DUTY}{min} – T_{CK2OUT}{max}	27 MHz	37.0 ns	12.3 ns
			74.25 MHz	13.5 ns	2.9 ns
	T_{HD}	Hold Time from ODCK = T_{CK2OUT}{min}	27 MHz	37.0 ns	0.4 ns
			74.25 MHz	13.5 ns	0.4 ns

Pin Descriptions

MHL/HDMI Receiver Input Port Pins

Pin Name	Pin	Type	Dir	Description
RXCN	2	TMDS	Input	HDMI Clock Pair. See the High-speed TMDS Signals section on page 46 for details.
RXCP	3	TMDS	Input	
RX0N	4	TMDS	Input	HDMI Channel 0 Pair or MHL Input Port Data pair In MHL mode, the other HDMI channels and clock pair are not used. See the High-speed TMDS Signals section on page 46 for details.
RX0P	5	TMDS	Input	
RX1N	6	TMDS	Input	HDMI Channel 1 Pair See the High-speed TMDS Signals section on page 46 for details.
RX1P	7	TMDS	Input	
RX2N	8	TMDS	Input	HDMI Channel 2 Pair See the High-speed TMDS Signals section on page 46 for details.
RX2P	9	TMDS	Input	
CBUS_HPD	21	Custom CBUS Schmitt 5 V tolerant	Input/ Output	In MHL mode, this pin is the Control Bus signal. The CBUS signal is for communication between the MHL transmitter and receiver using a 1.8 V signal level. In HDMI mode, this pin serves as the HPD out signal.
CBUS_OE	25	LVTTL	Output	Output enable for CBUS output
DSCL	20	Schmitt Open drain 5 V tolerant	Input/ Output	DDC I^2C Clock. HDCP KSV, An, and Ri values are exchanged over an I^2C port during authentication. DSCL drives low when only SBVCC5V or RPWR5V is present. More details refer to SiI9293 Application Notes. In MHL mode, this pin is used as DDC master to read EDID form the external EEPROM.
DSDA	19	Schmitt Open drain 5 V tolerant	Input/ Output	DDC I^2C Data. HDCP KSV, An, and Ri values are exchanged over an I^2C port during authentication. DSDA drives low when only SBVCC5V or RPWR5V is present. More details refer to SiI9293 Application Notes. In MHL mode, this pin is used as DDC master to read EDID form the external EEPROM.
CEC_A	26	CEC compliant 5 V tolerant	Input/ Output	HDMI compliant CEC I/O used to interface to CEC devices. This pin connects to the CEC signal of all HDMI connectors in the system. This pin has an internal pull-up resistor.

Digital Video Output Pins

Pin Name	Pin	Type	Dir	Description
Q0	37	LVTTL	Output	24-bit Output Pixel Data Bus. Q [23:0] is highly configurable using the various video configuration registers. It supports a wide array of output formats, including multiple RGB and YCbCr bus formats. Using the appropriate bits in the PD_SYS2 register, the output drivers can be put into a high impedance state. Refer to the Programmer's Reference for details.
Q1	38			
Q2	39			
Q3	40			
Q4	41			
Q5	42			
Q6	43			
Q7	44			
Q8	48			
Q9	49			
Q10	50			
Q11	51			
Q12	52			
Q13	53			
Q14	54			
Q15	55			
Q16	57			
Q17	58			
Q18	59			
Q19	60			
Q20	63			
Q21	64			
Q22	65			
Q23	66			
DE	35	LVTTL	Output	Data Enable.
HSYNC	36	LVTTL	Output	Horizontal Sync Output.
VSYNC	34	LVTTL	Output	Vertical Sync Output.
ODCK	46	LVTTL	Output	Output Data Clock.

Notes:

1. When transporting video data that uses fewer than 24 bits, the unused bits on the Q [23:0] bus can still carry switching pixel data signals. Unused Q [23:0] bus pins should be unconnected, masked or ignored by downstream devices. For example, carrying YCbCr 4:2:2 data with 16-bit width (see page 34), the bits Q [0] through Q [7] output switching signals.
2. The output data bus, Q [23:0], can be wire-ORed to another device so one device is always in the high-impedance state. However, these pins do not have internal pull-up or pull-down resistors, and so cannot pull the bus HIGH or LOW when all connected devices are in the high impedance state.

Digital Audio Output Pins

Pin Name	Pin	Type	Dir	Description
XTALIN	67	LVTTL 5 V tolerant	Input	Crystal Clock Input.
XTALOUT	68	LVTTL	Output	Crystal Clock Output.
MCLK	33	LVTTL	Output	Audio output Master Clock.
SCK	32	LVTTL	Output	I^2S or TDM Serial Clock.
WS	31	LVTTL	Output	I^2S word select or TDM Frame Start (FS) signal.
SD0_SPDIF	30	LVTTL	Output	I^2S/TDM serial data or S/PDIF audio output.

Note: The XTALIN pin can either be driven at LVTTL levels by a clock (leaving XTALOUT unconnected), or connected through a crystal to XTALOUT. Refer to Figure 6 on page 15.

Control and Configuration Pins

Pin Name	Pin	Type	Dir	Description
RESET_N	18	LVTTL Schmitt 5 V tolerant	Input	External Reset pin (Active low). This pin has an Internal pull-up. It can be left open when external reset is not required.
CSCL	14	LVTTL Schmitt Open drain 5 V tolerant	Input	Local I^2C Clock. This pin is true open drain, so it does not pull to ground if power is not applied. An external pull-up resistor to 3.3 V is required.
CSDA	13	LVTTL Schmitt Open drain 5 V tolerant	Input/ Output	Local I^2C Data. This pin is true open drain, so it does not pull to ground if power is not applied. An external pull-up resistor to 3.3 V is required.
TMODE	16	LVTTL Open Drain 5 V tolerant	Output	Test Mode Enable. Pull down for normal operation.
INT	15	LVTTL Open drain 5 V tolerant	Output	Active LOW interrupt output to host controller. This is an open drain output and requires an external pull-up resistor.
GPIO0_CI2CA	11	LVTTL Schmitt 5 V tolerant	Input/ Output	General Purpose I/O 0 or CI2CA. This pin defaults to an input and is sampled once at reset to select the local I^2C target address ranges. See the SiI9293 MHL/HDMI Receiver Programmer's Reference for details.
GPIO1	12	LVTTL Schmitt 5 V tolerant	Input/ Output	General Purpose I/O 1. See the SiI9293 MHL/HDMI Receiver Programmer's Reference for more details.
MHL_CD	24	LVTTL Schmitt 5 V tolerant	Input	MHL Cable Detect.

Power and Ground Pins

Pin Name	Pin	Type	Description
XTALVCC33	70	Power	XTAL Power 3.3 V.
XTALGND	69	Ground	XTAL Ground.
VDDH	1	Power	Receiver termination 3.3 V analog supply input. Connect to an external 3.3 V regulator or to VCC33_OUT as described below.
VDD	10,27,56	Power	Digital Power. 1.0 V.
APLLVDD	71	Power	Analog PLL Power. 1.0 V.
AVDD	72	Power	Analog Core VDD. 1.0 V.
VDDIO	29,47,62	Power	Digital IO Power. 3.3 V.
GNDIO	28,45,61	Ground	Digital IO Ground.
RPWR5V	22	Power	5 V Port Detection Input. Connect this pin to the HDMI +5 V input or VBUS +5 V input from the input MHL/HDMI connector. This pin requires a 10 Ω series resistor, a 5.1 KΩ pull-down resistor, and at least a 1 uF capacitor to ground. See Figure 27 on Page 44 for more details.
SBVCC5V	23	Power	Local Power 5 V Input. If there is no RPWR5V input, an active 5 V power input of this pin is required. This pin requires a 10 Ω series resistor.
VCC33_OUT	17	Power	Internal 3.3 V regulator output. This pin requires a 10 µF capacitor to ground. Maximum output current is 30 mA.
GND	ePad	Ground	Ground. All ground connections to the device are through the ePad, therefore it must be soldered to the board and the pad must have a low resistance connection to the board ground plane.

Feature Information

MHL 24-bit Mode

In 24-bit mode, MHL uses a single differential channel to transport TMDS data that encoded with 24 bits per pixel (three logic channels). One period of the MHL clock equals one clock period of the pixel clock, a period in which three TMDS characters are transmitted. The SiI9293 receiver supports up to 1080p30 video input in 24-bit mode

MHL Packed Pixel Mode

Packed Pixel mode allows 16 bits of data to be encoded and transmitted rather than the 24 bits per pixel in the 24-bit mode. The incoming pixel clock rate may be as high as 150 MHz in this mode for the MHL clock rate is half of the pixel clock. Only YCbCr 4:2:2 8-bit format is supported in Packed Pixel mode. The SiI9293 receiver supports up to 1080p60 / 3D 1080p30 in Packed Pixel mode. The Packed Pixel mode encoding should be indicated by the value accurately set in the CLK_MODE fields of the Status Registers. For details, refer to MHL Specification.

3D Video Formats

The SiI9293 receiver has support for the 3D video modes described in the HDMI 1.4 Specification and MHL 2 Specification. All modes support RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color formats and the 8- bit data width per color component. Table 21 and Table 22 show only the maximum possible resolution with a given frame rate; for example, Side-by-Side (Half) mode is defined for 1080p30, which implies that 720p60 and 480p60 are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

Table 21. Supported HDMI 3D Video Formats

HDMI 3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	24/30	148.5
		720p/1080i	50/60	
Side-by-Side	Full	1080p	24/30	
		720p/1080i	50/60	
	Half	1080p	50/60	
Top-and-Bottom	—	1080p	50/60	
		1080p	24/30	74.25
		720p/1080i	50/60	
Line Alternative	—	1080p	24/30	148.5
		720p/1080i	50/60	
Field Alternative	—	1080i	50/60	
L + Depth	—	1080p	24/30	
		720p/1080i	50/60	

For the supported MHL 3D formats listed in Table 22, the MHL 3D format is converted to the corresponding HDMI 3D format before being output by the SiI9293 receiver.

Table 22. Supported MHL 3D Video Formats

MHL 3D Format	Corresponding HDMI Format	Resolution	Frame Rate (Hz)	Input Link Clock for 8-bit Color (MHz)
Top-Bottom	Top-and-Bottom	1080p	50/60	74.25 (PackedPixel)
		720p/1080i	50/60	74.25
		1080p	24/30	
Left-Right	Side-by-Side (Half)	1080p	50/60	74.25 (PackedPixel)
		720p/1080i	50/60	74.25
		1080p	24/30	74.25
Frame Sequential	Frame Packing	720p	50/60	74.25 (PackedPixel)
		1080p	24/30	

Audio Output Interface

S/PDIF

The S/PDIF stream can carry two-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multichannel (IEC 61937) formats. The audio data output logic forms the audio data output stream from the HDMI audio packets. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes. Coherent means that the MCLK and S/PDIF are created from the same clock source.

I^2S

The I^2S bus format is programmable through registers, to allow interfacing with I^2S audio DACs or audio DSPs with I^2S inputs. Refer to the SiI9293 MHL/HDMI Receiver Programmer's Reference for different options on the I^2S bus. Additionally, the MCLK (audio master clock) frequency is selectable to be an integer multiple of the audio sample rate Fs.

MCLK frequencies support various audio sample rates, as shown in Table 23.

Table 23. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs : I^2S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	—	—
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz	—	—

TDM

Serial audio interfaces such as I^2S and TDM consist of words and channels (or slots), as shown in Figure 18.

HDMI and MHL allow 24-bit word. The TDM allows 32-bit channel. Each channel has up to 24-bit audio word and zero pads for the rest. The TDM frame can has 2/4/6/8-channel. TDM FS (Frame Start) identifies the first channel of the TDM frame, as shown in Figure 19.

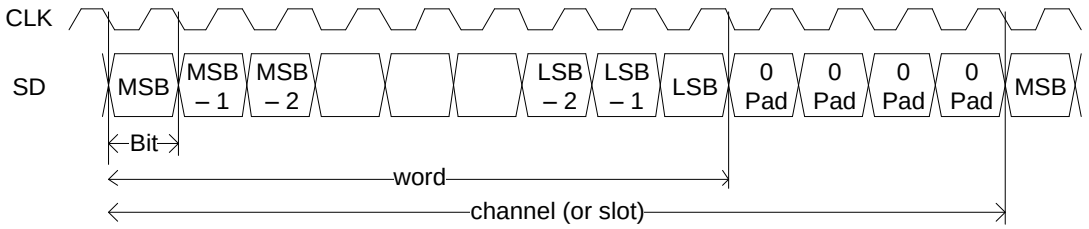


Figure 18. Word and Channel in TDM Audio Interface

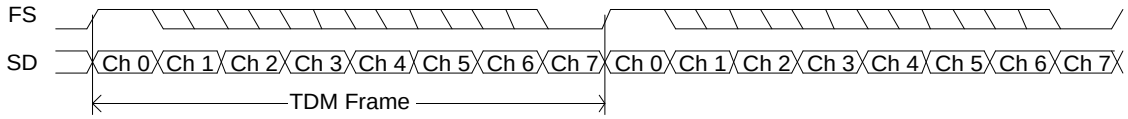


Figure 19. TDM Frame

In TDM, the first channel MSB has a one bit delay to FS. To cover the compliance issues, we have three options between the MSB of the first channel and FS: No delay, 1-bit delay, or 2-bit delay, as shown in Figure 20.
The control registers of the TDM share I^2S. Refer to the associated Programmer's Reference for information on these registers.

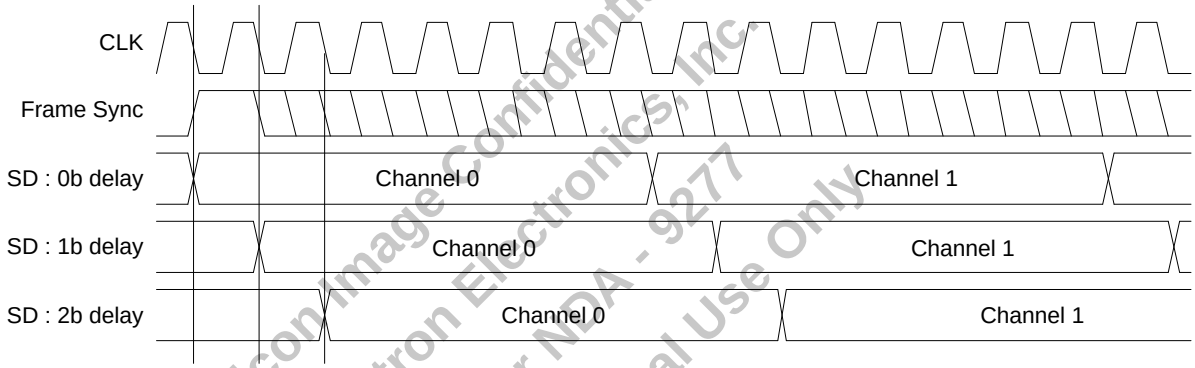


Figure 20. TDM – Delay of First Channel MSB to FS

Device Address Configuration Using CI2CA

All Functions of the SiI9293 receiver are controlled and observed with I^2C registers. The GPIO0_CI2CA pin defaults to an input CI2CA signal and is sampled once at reset to select the local I^2C target address ranges. Table 24 shows the device addresses as altered by the level of the CI2CA signal.

Table 24. Control of Transmitter I^2C Address with CI2CA Signal

Internal Function	Page Number	CI2CA = LOW	CI2CA = HIGH
System Control and Status	0	0x64	0x66
Analog Control Registers	1	0xD0	0xD0
Audio and AVI related Registers	2	0x68	0x68
VSI Control and Status	9	0xE0	0xE0
CEC	8	0x80	0x80
CBUS	C	0xC0	0xC0
Reserved for future use	—	0x72	0x72
	—	0x7A	0x7A
	—	0x92	0x92
	—	0x9A	0x9A

The Addresses for Pages 1, 2, and 9 are programmable. Refer to the Programmer's Reference for details.

Video Output Mode Configuration

The SiI9293 receiver supports multiple output data mappings. Some have separate control signals while some have embedded control signals. The selection of data mapping mode should be consistent at the pins and in the corresponding register settings. Refer to the SiI9293 MHL/HDMI Receiver Programmer's Reference for more details.

Table 25. Output Video Formats

Output Mode	Data Widths	Pixel Replication	Syncs	Page	Notes
RGB 4:4:4	24	1x	Separate	33	3, 7
YCbCr 4:4:4	24	1x	Separate	33	1. 3. 7
YCbCr 4:2:2 Sep. Syncs	16,20,24	1x	Separate	34	2, 3
YCbCr 4:2:2 Sep. Syncs	16,20,24	2x	Separate	34	2, 3, 8
YCbCr 4:2:2 Emb. Syncs	16,20,24	1x	Embedded	36	2, 5
YCbCr MUX 4:2:2	8,10,12	2x	Separate	38	2, 4, 8
YCbCr MUX 4:2:2 Emb. Syncs	8,10,12	2x	Embedded	40	2, 5, 6, 8, 9

Notes:

1. YCbCr 4:4:4 data contains one Cr, one Cb and one Y value for every pixel.
2. YCbCr 4:2:2 data contains one Cr and one Cb value for every two pixels; and one Y value for every pixel.
3. These formats can be carried across the HDMI link. Refer to the HDMI Specification 1.4, Section 6.2.3. The link clock must be within the specified range of the receiver.
4. In YC MUX mode data is sent to one or two 8/10/12-bit channels.
5. YC MUX with embedded SAV/EAV signal.
6. Syncs are embedded using SAV/EAV codes.
7. A 2x clock can also be sent with 4:4:4 data.
8. When sending a 2x clock, the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to the HDMI Specification 1.4, Section 6.4.
9. 2x clocking does not support YCbCr 4:2:2 embedded Sync timings for 720p or 1080i, as the output clock frequency would exceed the range allowed for the receiver.

The SiI9293 receiver can output video in various formats on its parallel digital output bus. Some transformations of the data received over HDMI are necessary in some modes. Digital output is used with either YCbCr 4:4:4 or YCbCr 4:2:2 data.

The diagrams do not include separation of the audio and InfoFrame packets from the HDMI stream, which occurs immediately after the TMDS and (optional) HDCP decoding. The HDMI link always carries separate HSYNC and VSYNC and DE. Therefore the SAV/EAV sync encoder must be used whenever the output mode includes embedded sync.

RGB and YCbCr 4:4:4 Formats with Separate Syncs

The pixel clock runs at the pixel rate and a complete definition of each pixel is output on each clock. Figure 21 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in Table 26. Figure 11 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 26. 4:4:4 Mappings

Pin Name	24-bit RGB	24-bit YCbCr
Q0	B0	Cb0
Q1	B1	Cb1
Q2	B2	Cb2
Q3	B3	Cb3
Q4	B4	Cb4
Q5	B5	Cb5
Q6	B6	Cb6
Q7	B7	Cb7
Q8	G0	Y0
Q9	G1	Y1
Q10	G2	Y2
Q11	G3	Y3
Q12	G4	Y4
Q13	G5	Y5
Q14	G6	Y6
Q15	G7	Y7
Q16	R0	Cr0
Q17	R1	Cr1
Q18	R2	Cr2
Q19	R3	Cr3
Q20	R4	Cr4
Q21	R5	Cr5
Q22	R6	Cr6
Q23	R7	Cr7
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC
DE	DE	DE

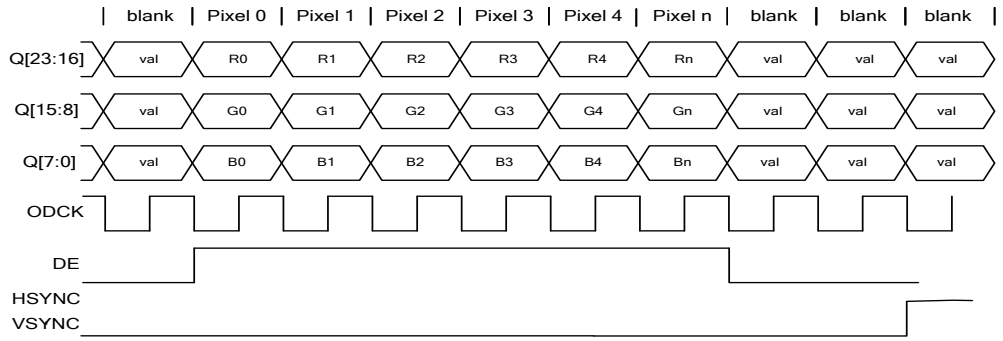


Figure 21. 4:4:4 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9293 registers, because no pixel data is carried on HDMI during blanking.

YCbCr 4:2:2 Formats with Separate Syncs

The YCbCr 4:2:2 formats output one pixel for every pixel clock period. A luminance (Y) value is sent for every pixel, but the chrominance values (Cb and Cr) are sent over two pixels. Pixel data can be 24-bit, 20-bit or 16-bit. HSYNC and VSYNC are output separately on their own pins. The DE HIGH time must contain an even number of pixel clocks. Figure 22. Figure 11 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 27. YCbCr 4:2:2 (Pass Through Only) Separate Sync Pin Mapping

Pin Name	16-bit YCbCr		20-bit YCbCr		24-bit YCbCr	
	Pixel 0	Pixel 1	Pixel 0	Pixel 1	Pixel 0	Pixel 1
Q0	NC	NC	NC	NC	Y0	Y0
Q1	NC	NC	NC	NC	Y1	Y1
Q2	NC	NC	Y0	Y0	Y2	Y2
Q3	NC	NC	Y1	Y1	Y3	Y3
Q4	NC	NC	NC	NC	Cb0	Cr0
Q5	NC	NC	NC	NC	Cb1	Cr1
Q6	NC	NC	Cb0	Cr0	Cb2	Cr2
Q7	NC	NC	Cb1	Cr1	Cb3	Cr3
Q8	Y0	Y0	Y2	Y2	Y4	Y4
Q9	Y1	Y1	Y3	Y3	Y5	Y5
Q10	Y2	Y2	Y4	Y4	Y6	Y6
Q11	Y3	Y3	Y5	Y5	Y7	Y7
Q12	Y4	Y4	Y6	Y6	Y8	Y8
Q13	Y5	Y5	Y7	Y7	Y9	Y9
Q14	Y6	Y6	Y8	Y8	Y10	Y10
Q15	Y7	Y7	Y9	Y9	Y11	Y11
Q16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Note: This pin mapping is only valid when the input video format is YCbCr 4:2:2 and the output video format is also YCbCr 4:2:2. No video processing block should be enabled when this pin mapping is used.

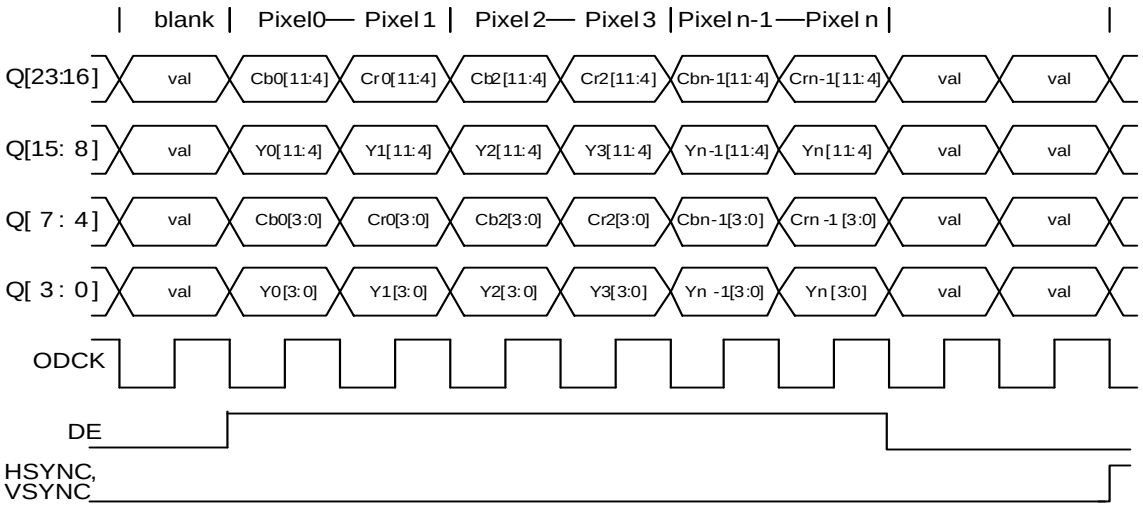


Figure 22. YCbCr Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9293 registers, because no pixel data is carried on HDMI during blanking.

YCbCr 4:2:2 Formats with Embedded Syncs

The YCbCr 4:2:2 embedded sync format is identical to the previous format (YCbCr 4:2:2), except that the syncs are embedded and not separate. Pixel data can be 24-bit, 20-bit, or 16-bit. DE is always output. Figure 23 shows the Start of Active Video (SAV) preamble, the End of Active Video" (EAV) suffix, and Figure 11 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 28. YCbCr 4:2:2 (Pass Through Only) Embedded Sync Pin Mapping

Pin Name	16-bit YCbCr		20-bit YCbCr		24-bit YCbCr	
	Pixel 0	Pixel 1	Pixel 0	Pixel 1	Pixel 0	Pixel 1
Q0	NC	NC	NC	NC	Y0	Y0
Q1	NC	NC	NC	NC	Y1	Y1
Q2	NC	NC	Y0	Y0	Y2	Y2
Q3	NC	NC	Y1	Y1	Y3	Y3
Q4	NC	NC	NC	NC	Cb0	Cr0
Q5	NC	NC	NC	NC	Cb1	Cr1
Q6	NC	NC	Cb0	Cr0	Cb2	Cr2
Q7	NC	NC	Cb1	Cr1	Cb3	Cr3
Q8	Y0	Y0	Y2	Y2	Y4	Y4
Q9	Y1	Y1	Y3	Y3	Y5	Y5
Q10	Y2	Y2	Y4	Y4	Y6	Y6
Q11	Y3	Y3	Y5	Y5	Y7	Y7
Q12	Y4	Y4	Y6	Y6	Y8	Y8
Q13	Y5	Y5	Y7	Y7	Y9	Y9
Q14	Y6	Y6	Y8	Y8	Y10	Y10
Q15	Y7	Y7	Y9	Y9	Y11	Y11
Q16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

Note: This pin mapping is only valid when the input video format is YCbCr 4:2:2 and the output video format is also YCbCr 4:2:2. No video processing block should be enabled when this pin mapping is used.

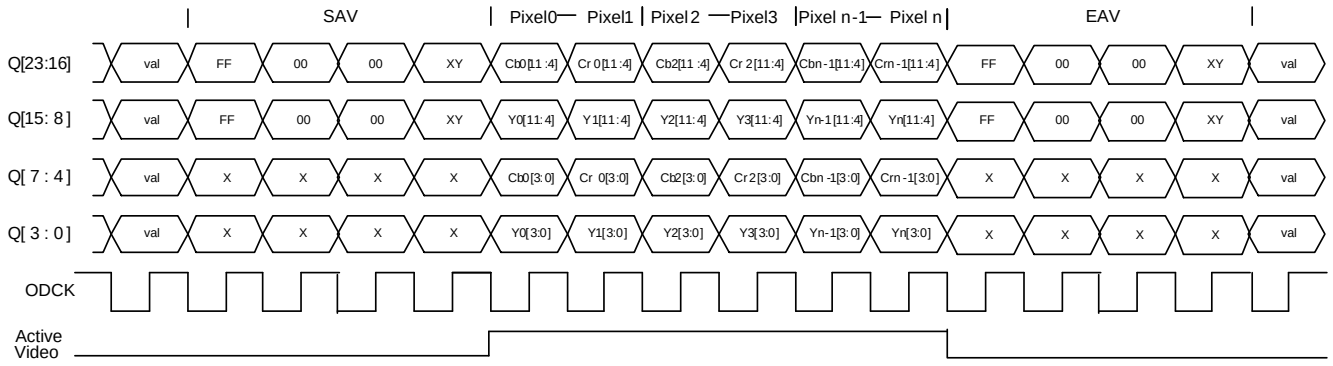


Figure 23. YCbCr 4:2:2 Embedded Sync Timing Diagram

Note: The val data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9293 registers, because no pixel data is carried on HDMI during blanking. SAV/EAV codes appear as an 8-bit field on both Q [23:16] (per SMPTE) and Q [15:8].

YCbCr Mux 4:2:2 Formats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping in Table 29, but complete luminance (Y) and chrominance (Cb and Cr) data is still provided for each pixel because the output pixel clock runs at twice the pixel rate. Figure 24 shows the 24-bit mode. The 16- and 20-bit mappings use fewer output pins for the pixel data. Note the separate syncs. Figure 11 shows OCLKDIV = 0 and OCKINV = 1.

Table 29. YCbCr Mux 4:2:2 Mappings

Pin Name	8-bit	10-bit	12-bit
	YCbCr	YCbCr	YCbCr
Q0	NC	NC	D0
Q1	NC	NC	D1
Q2	NC	D0	D2
Q3	NC	D1	D3
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	D0	D2	D4
Q9	D1	D3	D5
Q10	D2	D4	D6
Q11	D3	D5	D7
Q12	D4	D6	D8
Q13	D5	D7	D9
Q14	D6	D8	D10
Q15	D7	D9	D11
Q16	NC	NC	NC
Q17	NC	NC	NC
Q18	NC	NC	NC
Q19	NC	NC	NC
Q20	NC	NC	NC
Q21	NC	NC	NC
Q22	NC	NC	NC
Q23	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE

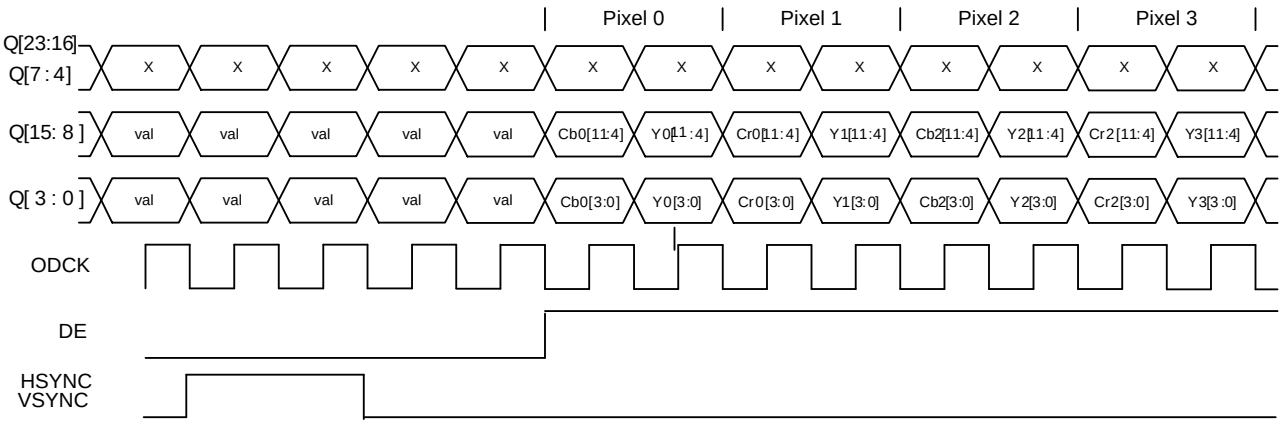


Figure 24. YCbCr Mux 4:2:2 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9293 registers, because no pixel data is carried on HDMI during blanking.

YCbCr Mux 4:2:2 Formats with Embedded Syncs

This mode is similar to YCbCr 4:2:2 with embedded syncs, but also multiplexes the luminance (Y) and chrominance (Cb and Cr) onto the same pins on alternating pixel clock cycles. Output clock rate is half the pixel clock rate on the link. SAV code is shown before rise of DE. EAV follows the falling edge of DE. See the ITU-R BT.656 Specification. 480p, 54-MHz output can be achieved if the input differential clock is 54 MHz. Figure 11 shows OCLKDIV = 0 and OCKINV = 1.

Table 30. YCbCr Mux 4:2:2 Embedded Sync Pin Mapping

Pin Name	8-bit	10-bit	12-bit
	YCbCr	YCbCr	YCbCr
Q0	NC	NC	D0
Q1	NC	NC	D1
Q2	NC	D0	D2
Q3	NC	D1	D3
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	D0	D2	D4
Q9	D1	D3	D5
Q10	D2	D4	D6
Q11	D3	D5	D7
Q12	D4	D6	D8
Q13	D5	D7	D9
Q14	D6	D8	D10
Q15	D7	D9	D11
Q16	NC	NC	NC
Q17	NC	NC	NC
Q18	NC	NC	NC
Q19	NC	NC	NC
Q20	NC	NC	NC
Q21	NC	NC	NC
Q22	NC	NC	NC
Q23	NC	NC	NC
HSYNC	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded

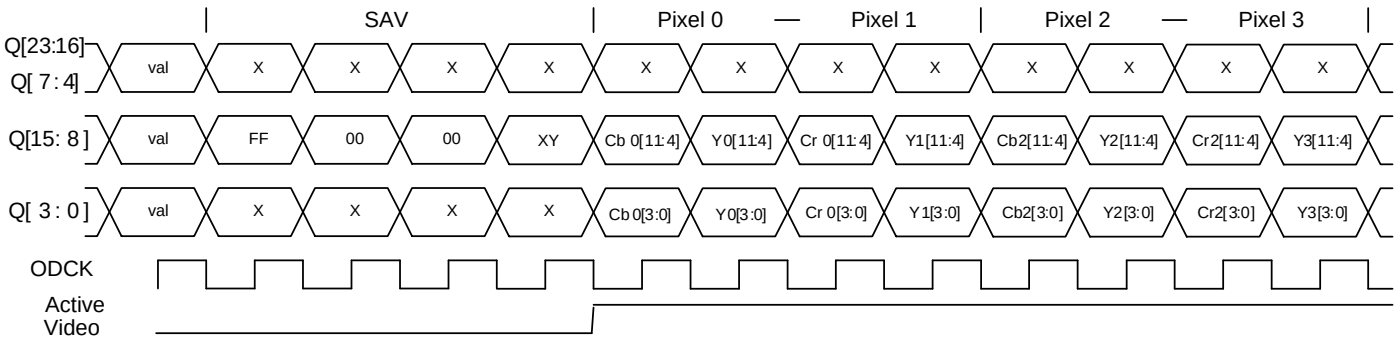


Figure 25. YCbCr Mux 4:2:2 Embedded Sync Encoding Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9293 registers, because no pixel data is carried on HDMI during blanking. Refer to the SiI9293 MHL/HDMI Receiver Programmer's Reference for details.

12-bit RGB and YCbCr 4:4:4 Formats with Separate Syncs

The output clock runs at the pixel rate and a complete definition of each pixel is output on each clock. One clock edge drives out half the pixel data on 12 pins. The opposite clock edge drives out the remaining half of the pixel data on the same 12 pins. Figure 26 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in the columns of Table 31. Control signals (DE, HSYNC, and VSYNC) change state with respect to the first edge of ODCK.

Table 31. 12-bit Output 4:4:4 Mappings

Pin Name	24-bit			
	RGB		YCbCr	
	First Edge	Second Edge	First Edge	Second Edge
Q0	B0	G4	Cb0	Y4
Q1	B1	G5	Cb1	Y5
Q2	B2	G6	Cb2	Y6
Q3	B3	G7	Cb3	Y7
Q4	B4	R0	Cb4	Cr0
Q5	B5	R1	Cb5	Cr1
Q6	B6	R2	Cb6	Cr2
Q7	B7	R3	Cb7	Cr3
Q8	G0	R4	Y0	Cr4
Q9	G1	R5	Y1	Cr5
Q10	G2	R6	Y2	Cr6
Q11	G3	R7	Y3	Cr7
Q12	NC	NC	NC	NC
Q13	NC	NC	NC	NC
Q14	NC	NC	NC	NC
Q15	NC	NC	NC	NC
Q16	NC	NC	NC	NC
Q17	NC	NC	NC	NC
Q18	NC	NC	NC	NC
Q19	NC	NC	NC	NC
Q20	NC	NC	NC	NC
Q21	NC	NC	NC	NC
Q22	NC	NC	NC	NC
Q23	NC	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE

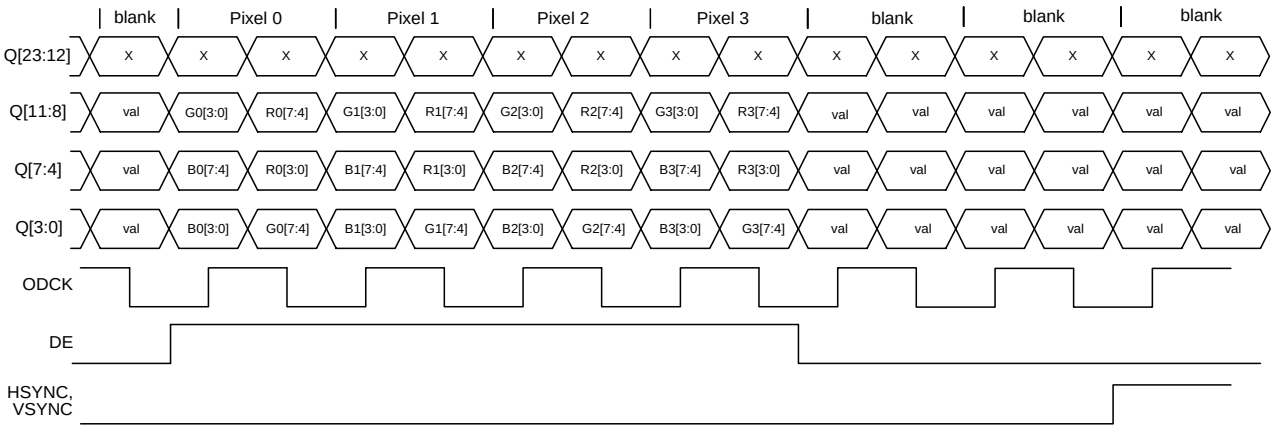


Figure 26. 12-bit Output RGB Timing Diagram

System Design Guidelines

The tolerance of all resistors shown in this section is ± 5% unless otherwise noted.

HDMI/MHL Design Application

Figure 27 shows a sample design circuit for MHL and HDMI connection. Refer to SiI9293 Application Notes for more details.

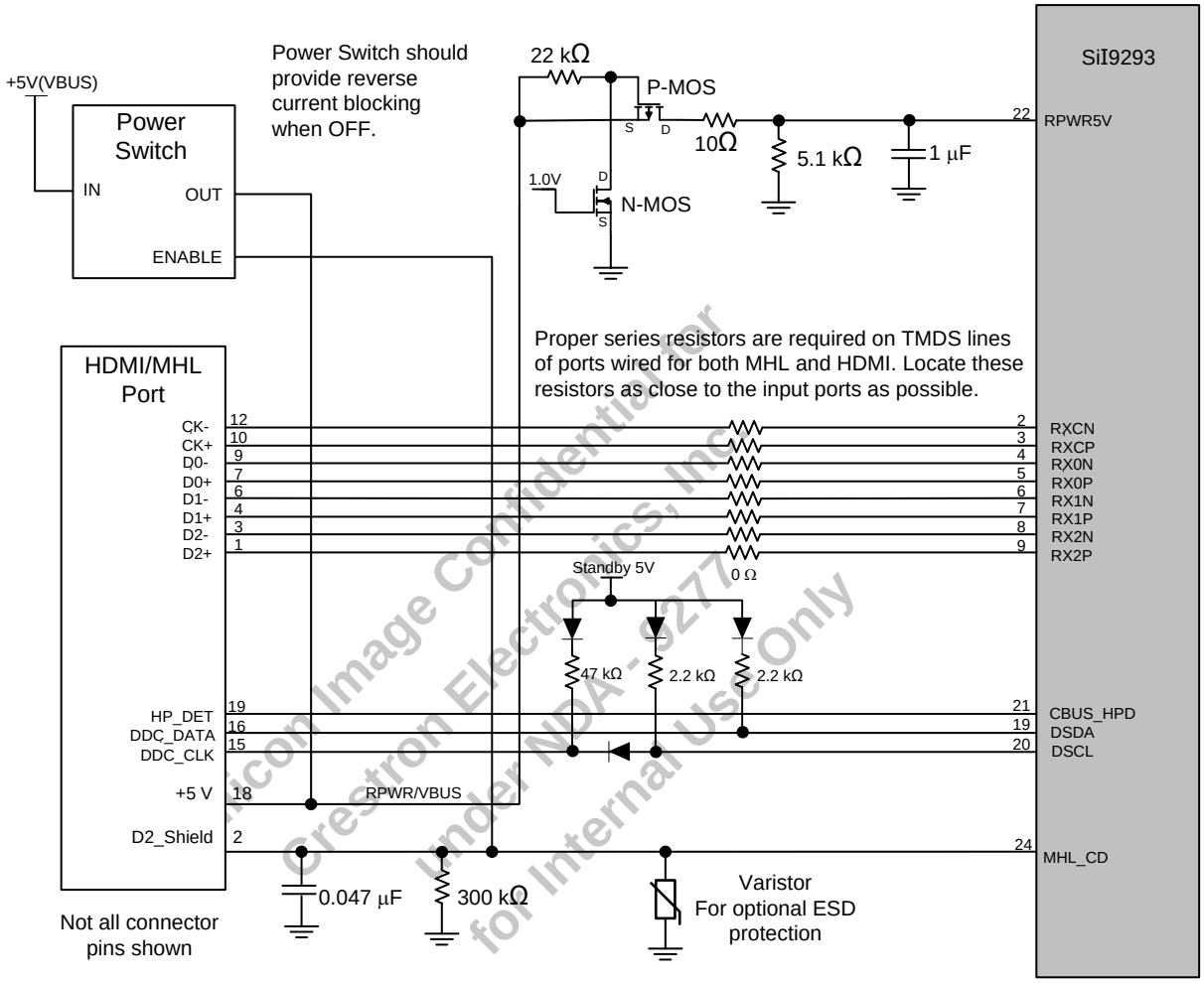


Figure 27. Connection of MHL and HDMI Port

Power Supply Decoupling

Silicon Image recommends that designers include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 28. Place these components as close as possible to the SiI9293 device pins and avoid routing traces through vias, if possible. An example of this layout configuration is shown in Figure 29. Connections in one group (such as VDD) can share C2, C3, and L1, with each pin having a separate C1 placed as close as possible to the pin. Suggested values for C1, C2 and C3 are 0.01 µF, 0.1 µF, and 10 µF, respectively. The recommended impedance of ferrite L1 is 10 Ω or more in the frequency range of 1 – 2 MHz for all power supplies.

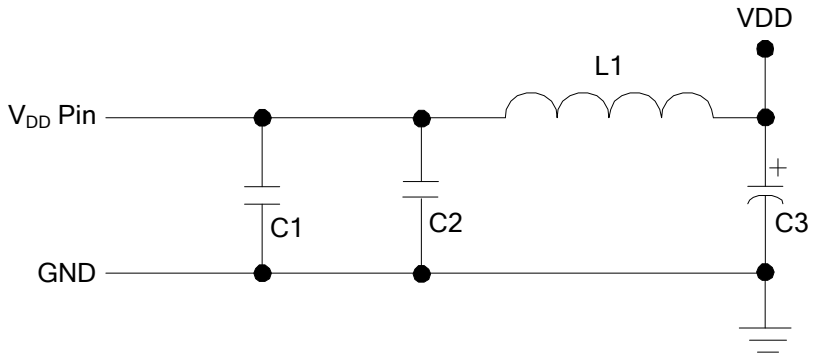


Figure 28. Decoupling and Bypass Schematic

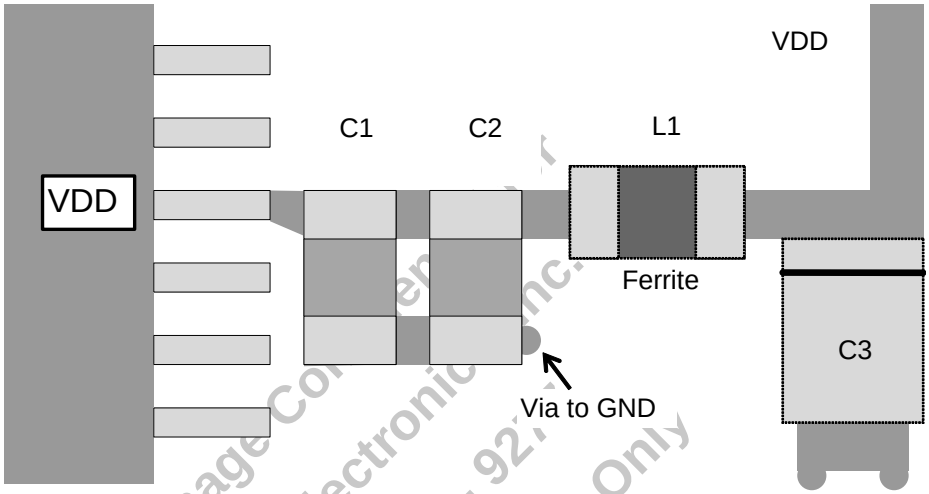


Figure 29. Decoupling and Bypass Capacitor Placement

High-speed TMDS Signals

Layout Guidelines

The SiI9293 device should be placed as closed as possible to the MHL/HDMI input connector. The differential lines should be routed as directly as possible from the SiI9293 receiver to connector. Silicon Image devices are tolerant of skews between input differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together. Passing the TMDS lines through vias is not recommended. Locate the ESD protection diodes as close as possible to the MHL connector. Each pair of differential traces should have 100 Ω differential impedance, and the MHL differential pair traces should have 30 Ω common mode impedance.

Termination Requirement

A 0 Ω resistor, shown as *R* in Figure 30, must be placed in series with all TMDS receiver pins. In addition, the distance from the resistor to the TMDS receiver pins, designated as *d* in the figure, must be within 1 cm or 393 mils, to ensure the impedance does not deviate from the limits allowed by the MHL 2 Specification.

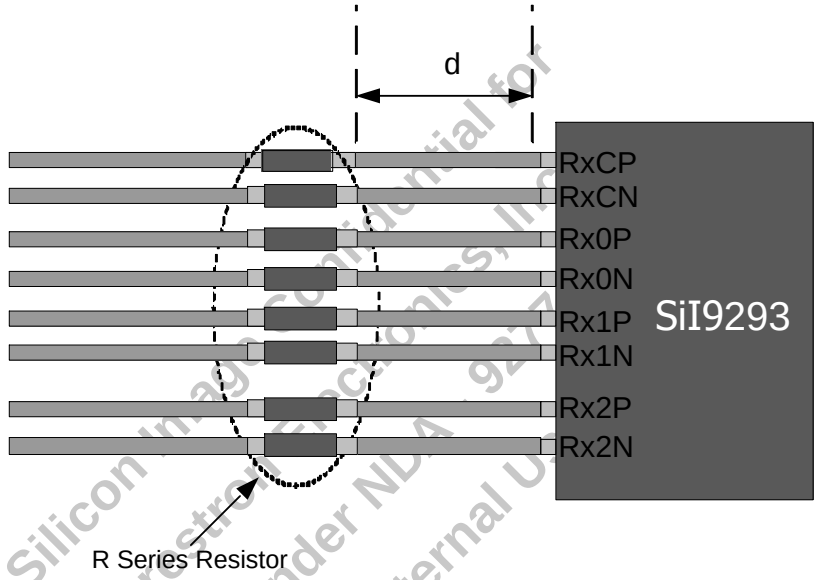


Figure 30. TMDS Signal Termination

ESD Protection

The SiI9293 receiver can withstand electrostatic discharges due to handling during manufacture. In applications where higher protection levels are required, ESD-limiting components can be placed on the differential lines of the chip. These components typically have a capacitive effect that reduces the signal quality at higher clock frequencies. Use the lowest capacitance devices possible. ESD components must be placed after the series termination resistors and as close as possible to the input or output connector. In no case can the capacitance value of these components exceed 1 pF.

EMI Considerations

Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines, except the common-mode chokes and ESD protection described earlier. The differential signaling used in HDMI is inherently low in EMI if the routing recommendations noted in the Layout Guidelines section on page 46 are followed.

The PCB ground plane should extend unbroken under as much of the transmitter chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

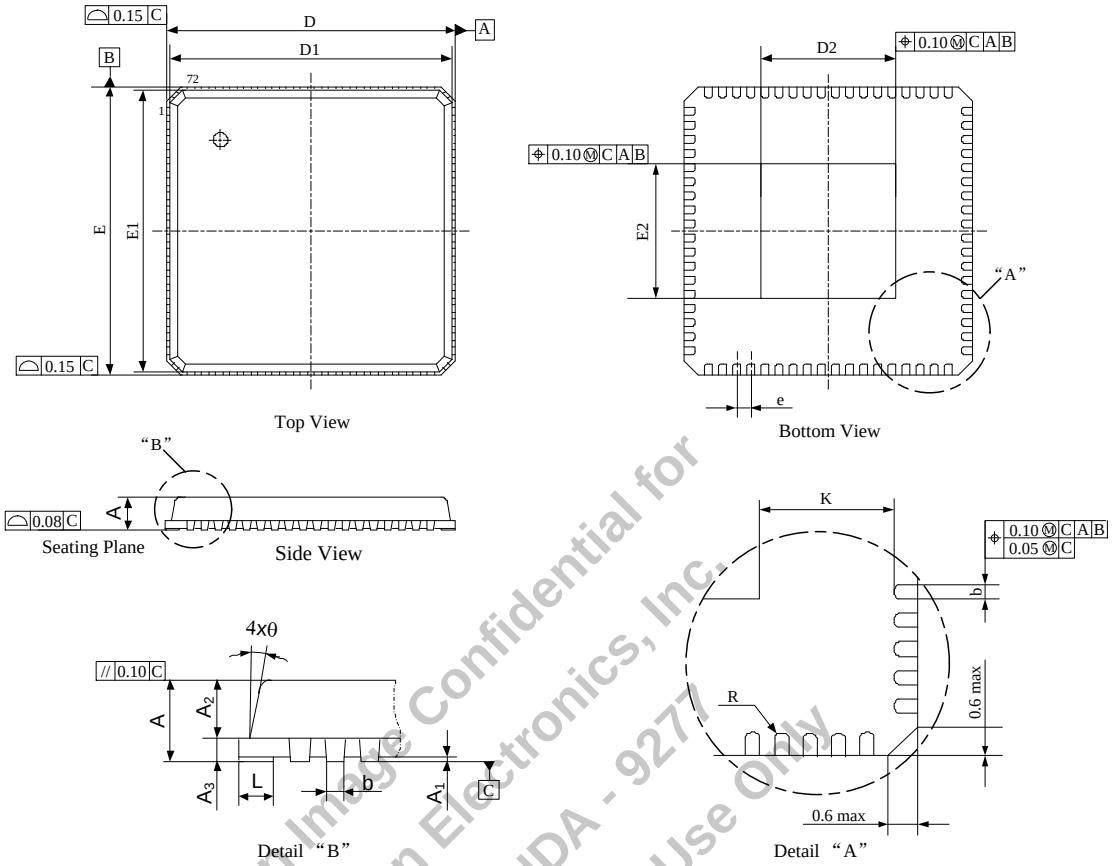
Packaging

ePad Requirements

The SiI9293 MHL/HDMI Receiver chip is packaged in a 72-pin QFN package with an Exposed Pad™ (ePad™) that is used for electrical ground of the device and for improving thermal transfer characteristics. The ePad dimensions are 4.7 mm x 4.7 mm shown on the following page. Soldering the ePad to the ground plane of the PCB is ***required*** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. As a general guideline, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical short. Figure 31 shows the package dimensions of the SiI9293 MHL/HDMI Receiver.

Package Dimensions

Package drawings are not to scale.



JEDEC Package Code MO-220

Symbol	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A_1	Stand-off	0.00	0.02	0.05
A_2	Body thickness	0.60	0.65	0.70
A_3	Base thickness	0.20 REF		
D / E	Body size	10.00 BSC		
D1 / E1	Body size	9.75 BSC		
D2 / E2	ePad size	4.55	4.70	4.85
b	Plated lead width	0.18	0.23	0.28
e	Lead pitch	0.50 BSC		
L	Lead foot length	0.30	0.40	0.50
θ	Mold angle	0 °	—	14 °
R	Lead tip radius	0.09	—	—
K	Lead to ePad clearance	0.20	—	—

All dimensions are in millimeters.

Figure 31. 72-pin QFN Package Diagram

Marking Specification

Marking drawing is not to scale.

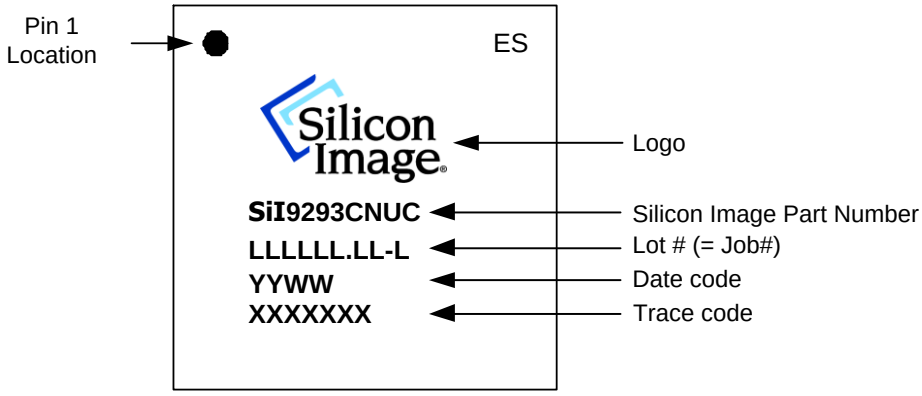


Figure 32. Marking Diagram

Ordering Information

Production Part Numbers:

Device	Part Number
SiI9293 MHL/HDMI receiver	SiI9293CNUC

The universal package can be used in lead-free and ordinary process lines.

References

Standards Documents

Table 32 lists the abbreviations used in this document. Contact the responsible standards groups listed in Table 33 for more information on these specifications.

Table 32. Referenced Documents

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface, Revision 1.4b*, HDMI Consortium, October 2011
HCTS	*HDMI Compliance Test Specification, Revision 1.4b*, HDMI Consortium, October 2011
HDCP	*High-bandwidth Digital Content Protection, Revision 1.4*, Digital Content Protection, LLC, July 2009
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA; Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, March 2001
CEA-861-E	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, EIA/CEA, March 2008
EDDC	*Enhanced Display Data Channel Standard, Version 1.1*, VESA; March 2004
I^2C	*The I^2C Bus Specification*, Version 2.1, Philips Semiconductors, January 2000
MHL	*MHL (Mobile High-definition Link) Specification*, Version 2.0, MHL, LLC, June 2012

Table 33. Standards Groups Contact Information

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
I^2C	http://www.nxp.com	—	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—
MHL	http://www.mhlconsortium.org	Customerservice@mhlconsortium.org	408-962-4269

Silicon Image Documents

Table 34 lists Silicon Image documents that are available from your Silicon Image sales representative.

Table 34. Silicon Image Publications

Document	Title
SiI-PR-1066	*SiI9293 MHL/HDMI Receiver*

Disclaimers

These materials are provided on an "AS IS" basis. Silicon Image, Inc. and its affiliates disclaim all representations and warranties (express, implied, statutory or otherwise), including but not limited to: (i) all implied warranties of merchantability, fitness for a particular purpose, and/or non-infringement of third party rights; (ii) all warranties arising out of course-of-dealing, usage, and/or trade; and (iii) all warranties that the information or results provided in, or that may be obtained from use of, the materials are accurate, reliable, complete, up-to-date, or produce specific outcomes. Silicon Image, Inc. and its affiliates assume no liability or responsibility for any errors or omissions in these materials, makes no commitment or warranty to correct any such errors or omissions or update or keep current the information contained in these materials, and expressly disclaims all direct, indirect, special, incidental, consequential, reliance and punitive damages, including WITHOUT LIMITATION any loss of profits arising out of your access to, use or interpretation of, or actions taken or not taken based on the content of these materials.

Silicon Image, Inc. and its affiliates reserve the right, without notice, to periodically modify the information in these materials, and to add to, delete, and/or change any of this information.

Notwithstanding the foregoing, these materials shall not, in the absence of authorization under U.S. and local law and regulations, as required, be used by or exported or re-exported to (i) any U.S. sanctioned or embargoed country, or to nationals or residents of such countries; or (ii) any person, entity, organization or other party identified on the U.S. Department of Commerce's Denied Persons or Entity List, the U.S. Department of Treasury's Specially Designated Nationals or Blocked Persons List, or the Department of State's Debarred Parties List, as published and revised from time to time; (iii) any party engaged in nuclear, chemical/biological weapons or missile proliferation activities; or (iv) any party for use in the design, development, or production of rocket systems or unmanned air vehicles.

Products and Services

The products and services described in these materials, and any other information, services, designs, know-how and/or products provided by Silicon Image, Inc. and/or its affiliates are provided on as "AS IS" basis, except to the extent that Silicon Image, Inc. and/or its affiliates provides an applicable written limited warranty in its standard form license agreements, standard Terms and Conditions of Sale and Service or its other applicable standard form agreements, in which case such limited warranty shall apply and shall govern in lieu of all other warranties (express, statutory, or implied). EXCEPT FOR SUCH LIMITED WARRANTY, SILICON IMAGE, INC. AND ITS AFFILIATES DISCLAIM ALL REPRESENTATIONS AND WARRANTIES (EXPRESS, IMPLIED, STATUTORY OR OTHERWISE), REGARDING THE INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS PROVIDED BY SILICON IMAGE, INC. AND/OR ITS AFFILIATES, INCLUDING BUT NOT LIMITED TO, ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND/OR NON-INFRINGEMENT OF THIRD PARTY RIGHTS. YOU ACKNOWLEDGE AND AGREE THAT SUCH INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS HAVE NOT BEEN DESIGNED, TESTED, OR MANUFACTURED FOR USE OR RESALE IN SYSTEMS WHERE THE FAILURE, MALFUNCTION, OR ANY INACCURACY OF THESE ITEMS CARRIES A RISK OF DEATH OR SERIOUS BODILY INJURY, INCLUDING, BUT NOT LIMITED TO, USE IN NUCLEAR FACILITIES, AIRCRAFT NAVIGATION OR COMMUNICATION, EMERGENCY SYSTEMS, OR OTHER SYSTEMS WITH A SIMILAR DEGREE OF POTENTIAL HAZARD. NO PERSON IS AUTHORIZED TO MAKE ANY OTHER WARRANTY OR REPRESENTATION CONCERNING THE PERFORMANCE OF THE INFORMATION, PRODUCTS, KNOW-HOW, DESIGNS OR SERVICES OTHER THAN AS PROVIDED IN THESE TERMS AND CONDITIONS.

1140 E. Arques Avenue
Sunnyvale, CA 94085
T 408.616.4000 F 408.830.9530
www.siliconimage.com

1140 E. Arques Avenue
Sunnyvale, CA 94085
T 408.616.4000 F 408.830.9530
www.siliconimage.com